MODULE 2

DIGITAL VOLTMETERS

The digital voltmeters referred as DVM, converts the analog signals into digital and display the voltages to be measured as discrete numerals rather than pointer deflection, on the digital displays.

DVMs can be used to measure a.c. and d.c. voltages and with proper transducer and signal conditioning circuit it can also measure parameters like pressure, temperature, stress etc.

The output voltage is displayed on the digital display on the front panel.

These DVMs reduces the human reading and interpretation errors and parallax errors. The DVMs have various features and the advantages, over the conventional analog voltmeters having pointer deflection on the continuous scale.

There are different types of DVM which differ in number of digits, accuracy, speed of reading, size, power requirements and cost.

The important performance characteristics of DVM are as follows:
1. The input ranges from 1v to 1000v with provision for range selection and also indicates the overload condition.
2. Accuracy is high as ±0.005% of reading
3. Resolution is 1ppm i.e the meter can read 1μv on a 1V range
4. Input impedance is around 10MΩ which helps in reducing loading effect.
5. Output is in BCD form and for other forms of output digital processing modules can be included.

Ramp Technique:

The basic principle is based on measuring the time taken by linear ramp change input level to ground level or vice-versa. This time is measured with the help of electronic time interval counter and the count is displayed in the numeric form with the help of a digital display. This measured value is proportional to the input. Block diagram and operation principle is shown in the below figures.

- At the start of measurement, a ramp voltage is initiated along with resetting the counter by a multivibrator.
- The ramp voltage generated is continuously compared with the input voltage by the input comparator and when both these voltages equals, the comparator generates a 'start' pulse which opens/enables the gate.
- The ramp continues to decrease and finally reaches to 0 V or ground potential and this is sensed by the second comparator or ground comparator.
- As soon as the gate is enabled the oscillator circuit drives the counter and the counter starts counting.
- When the ramp voltage is exactly 0V, the ground comparator produces a ‘stop’ pulse which closes/disables the gate.
- From the time the gate is enabled to disabled, the number of clock pulses are measured by the counter and this time duration for which the gate is enabled, is proportional to the input voltage.
- The magnitude of the count indicates the magnitude of the input voltage, which is displayed by the display. The block diagram of linear ramp DVM is shown in the Fig

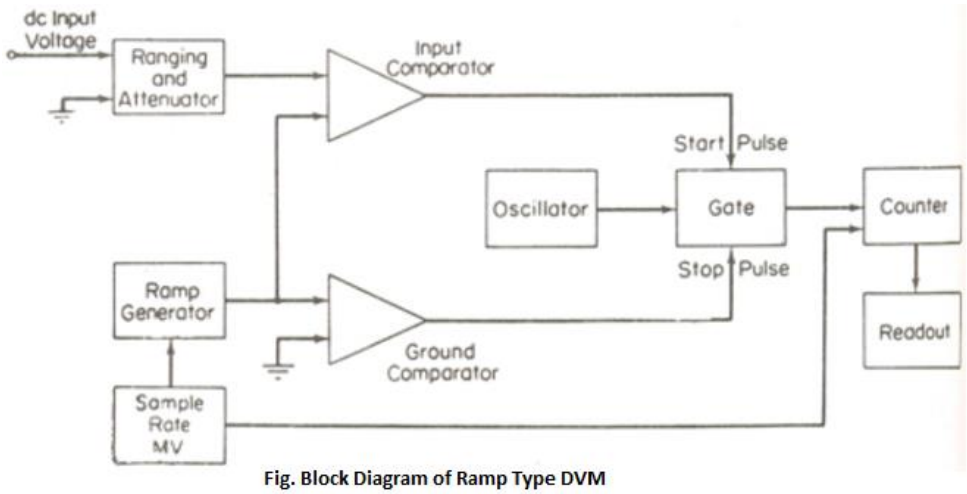


Fig. Block Diagram of Ramp Type DVM

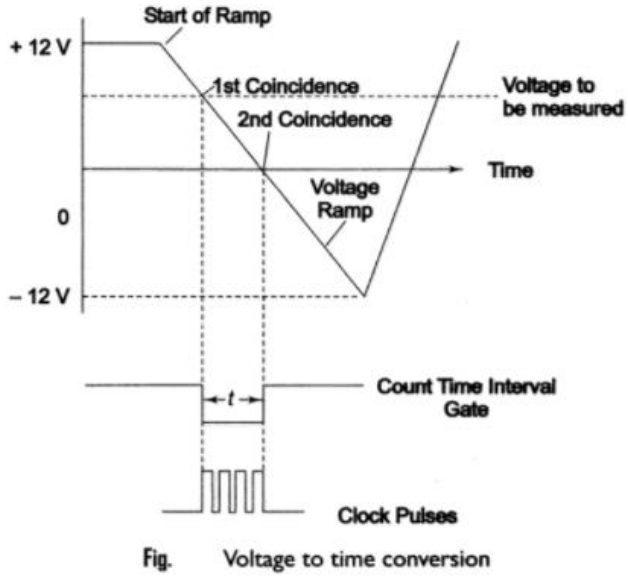


Fig. Voltage to time conversion

Advantages:

- Easy to design
- Low cost
- Output pulses can be transmitted over longer feeder lines

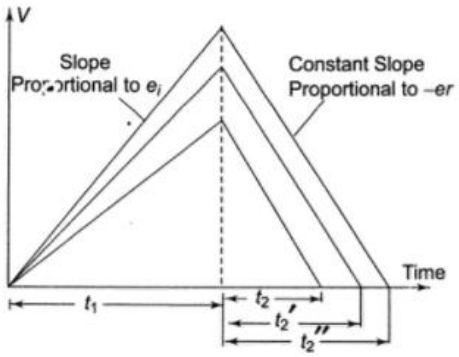
Disadvantages:

- Ramp generator requires excellent characteristics related to linearity
- Large errors are possible when noise is super imposed on the input signal.

Dual Slope DVM: (Voltage to Time conversion)

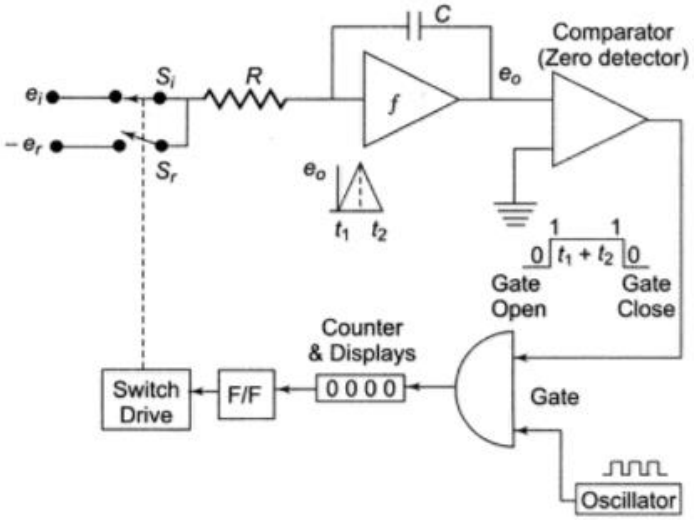
Operating Principle:

The basic principle of this method is that the input signal is integrated for a fixed interval of time. And then the same integrator is used to integrate the reference voltage with reverse slope. Hence which is constant and proportional to the magnitude of the input. Thus the name given to the technique is **dual slope** integration technique. This is shown in the figure below.



Basic principle of dual slope type DVM

The block diagram of dual slope integrating type DVM is shown in the Fig.



Block diagram of a dual slope type DVM

- At the start, a pulse resets the counter and the flip-flop and this makes the switch Si to close and switch Sr to open.
- The input ei appears at the integrator and the capacitor C begins to charge. As the output of the integrator exceeds 0, the comparator output is changed to 1 and this enables the gate. This causes the clock pulses to feed the counter.
- The counter starts counting until it reaches it maximum count i.e 9999. The time taken for this is denoted as t1. During this time the capacitor is charged to the input ei.
- Upon max count value at the counter and for the next clock pulse the counter value will be 0000 with a carry which is fed to the flip-flop. This drives the switch Sr to close and Si is now open.
- With this now –er (-ve reference) is given to the integrator. Now the capacitor begins to discharge causing output of integrator to decrease. At some time instant t2, the integrator output reaches 0 and this cause the comparator to change its state to 0. This disables the gate.
- During time t2, the capacitor discharges with a constant slope and this is proportional to the input voltage.
- When the counter stops counting the pulses, the value has a direct relation with the input voltage and it is given by,
  During charging of capacitor, i.e during time t1, the output of integrator is given by,

$$e_0 = \frac{-1}{RC}\int_0^{t1} ei\ dt = \frac{-ei*t1}{RC} \text{ ----------(1)}$$

During Discharging of capacitor, i.e during time t2, the output is given by

$$e_0 = \frac{1}{RC}\int_0^{t2} -er\ dt = \frac{-er*t2}{RC} \text{ ----------(2)}$$

Subtracting (2) from (1)

$$e_0 - e_0 = \frac{-ei*t1}{RC} + \frac{er*t2}{RC}$$

$$\frac{ei*t1}{RC} = \frac{er*t2}{RC}$$

$$ei = er * \frac{t2}{t1} \text{ ----------(1)}$$

Suppose if the oscillator period is T and the counter indicates n1 and n2 counts, then

$$ei = er * \frac{n2 * T}{n1 * T}$$

$$ei = er * \frac{n2}{n1}$$

Now n1 and n2 are constants and considering variable K1 = er/n1 then we can write ei as

$$ei = K1 * n2 \text{ ----------(2)}$$

From eqn (1) and (2), it is clear that accuracy of measured value does not depend on the integrator time constant.
From eqn (2) it indicates that the accuracy is independent of the oscillatory frequency.

Advantages:

- It has excellent noise rejection and the noise is averaged out by the positive and negative ramps using the process of integration.
- Accuracy is ±0.005%

Disadvantage:

- The only disadvantage seen in this type DVM is that the process is slow

Integrating type DVM (Voltage to Frequency Converter):

Operating principle: In this a constant input voltage is integrated and the slope of the output ramp is proportional to the input voltage. When the output voltage reaches certain value, it discharges to 0 and the next cycle begins and this continues. Frequency of this output is proportional to the input voltage. The principle of conversion from voltage to frequency is shown in the fig.
The number of pulses appearing in a definite interval of time is counted and as the frequency of these pulses is a function of the unknown voltage, the number of pulses counted in that period of time is the indication of the unknown input voltage.

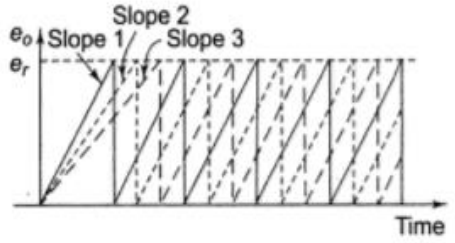


Fig. Voltage to frequency conversion

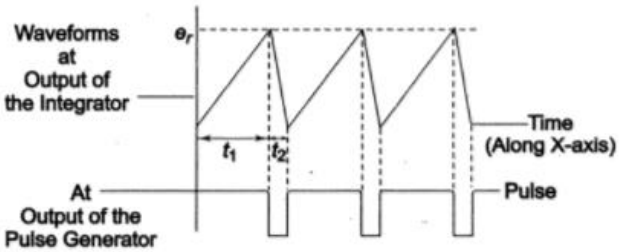


Fig.

- The heart of integrating type of DVM is the operational amplifier which used as an integrator. The block diagram of integrating ramp DVM is shown in fig. below.
- The input voltage ei, when applied generates a charging current ei/R which charges the capacitor to the reference voltage er.
- When the integrator output reaches er (i.e charging of capacitor to er) the comparator changes its state and this triggers the precision pulse generator.
- The precision pulse genertates a pulse of precison charge of negative polarity of the er and this rapidy discharge the capacitor. The output of integrator and pulse generated output waveform is showin in the above fig.
- As the capacitor discharges the output of integrator changes and causes the comparator to change its state bake to initial state and this cycle repeates.
- The rate of charging and discharging produces signal frequency that is directly proportional to input ei.

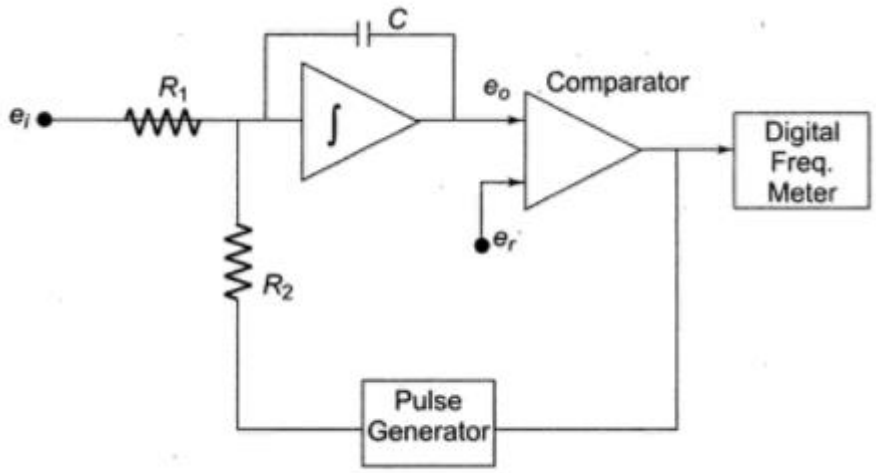


Fig. Block diagram of an integrating type DVM

- The output expression for integrating type DVM is same as that of Dual Slope integrating, using the same we have,

$$ei = er * \frac{t2}{t1}$$

Here er and t2 are constants. Considering another variable K2 as
Let K2 = er *t2

$$ei = K2 * \frac{1}{t1}$$

Therefore we can say, $ei = k2 * f0$
Thus measured input is function of the frequency.

Advantages:

- This type of DVM is capable of giving accurate results even in the presence of noise.

Staircase Ramp Technique:

In this method the input signal is compared with an internally generated voltage which increases in steps from 0. The number of steps required to match both the inputs is counted.

Operation Principle: The input signal Vi is compared with internally generated staircase voltage Vc. As the inputs are not same at the begining a counter is initiated to count. The counter will count until Vi = Vc and then the counter is disabled. The counted valued is displayed which is proportional to the input Vi.

- The block diagram of staircase ramp type DVM is shown in Fig b
- At the initial step of measurement, the counter is reset to 0 and this counter output drives the Digital to Analog Converter (DAC). The output of DAC, which is an analog voltage is given as input to the comparator, denoted as Vc (this is the staircase voltage which is internally generated)
- Upon the application of Vc, the comparator changes its state to 1 and this enables the gate, which allows the clock pulses to the counter and the counter starts counting. This time is t1 (i.e gate is enabled at time t1)
- For each count at the counter, the DAC will generate corresponding analog voltages which increases in small amount. Thus the output of DAC is a staircase voltage as shown in Fig a.
- The process is repeated until the input voltage Vi equals the DAC voltage Vc(until this the gate is enabled and the counter will be counting) at the moment Vi = Vc the comparator changes its state to 0 and this disables the gate, thus blocking the clock pulses. The counter stops counting and the displayed value is proportional to the input value.

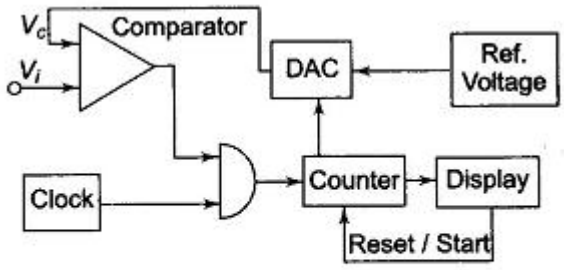


Fig. b Block Diagram of a Staircase Ramp Type

Advantages:

- Input impedance of the DAC is high when the compensation (Vi=Vc) is reached.
- The accuracy depends only on the stability and accuracy of the voltage and DAC. The clock has no effect on the accuracy.

Disadvantages:

- The system measures the instantaneous value of the input signal at the moment compensation is reached. This means the reading is rather unstable, i.e. the input signal is not a pure dc voltage.
- Until the full compensation is reached, the input impedance is low, which can influence the accuracy.

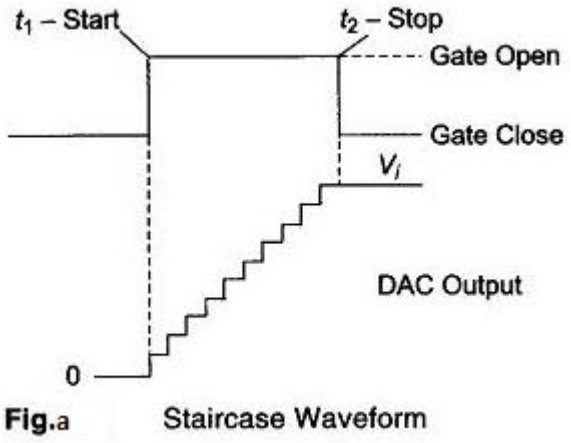


Fig.a Staircase Waveform

Successive Approximation Technique

The principle of successive approximations can be understood using a simple example of measuring the weight of an object using a balance. In the process an approximate weight is placed and then adding or removal of smaller weights is done for balancing. Or it uses the same principle used in binary search algorithm.

- The basic block diagram is shown in Fig.2.1.
- When the start pulse signal is given through multivibrator, the successive approximation register (SAR) is cleared.
- The output of the SAR is 00000000 which the input to DAC and thus Vout of the D/A converter is 0.
- When the input Vin is applied and during the first clock pulse, the control circuit sets the (MSB) D7 to 1. The SAR output is 10000000 and this causes the output of DAC, Vout to Vref/2.
- If Vin > Vout the comparator produces an output which retains the set state of D7.
- In the next pulse the ring counter in the block advances the count value and impends 1 in the next MSB position i.e D6. Now the SAR output is 11000000.
- The DAC now produces Vout as Vref/2+Vref/4 and this voltage is again compared with Vin.
- In the next pulse if Vin > Vout the D6 will be retained as set state and D5 will be set and SAR is now 11100000 and DAC produces output as Vref/2+Vref/4+Vref/8.

- Suppose if Vin is less than Vout the comparator produces an output which resets the D7 and the ring counter impends 1 to D6. The SAR is now 01000000. The DAC output is now Vref/4.

- This is compared with Vin. If still Vin < Vout D6 will be reset and D5 will be set by ring counter. SAR has now 00100000 and DAC output for this is Vref/8.

- The measurement cycle repeats and continues until ring counter reaches its max count.

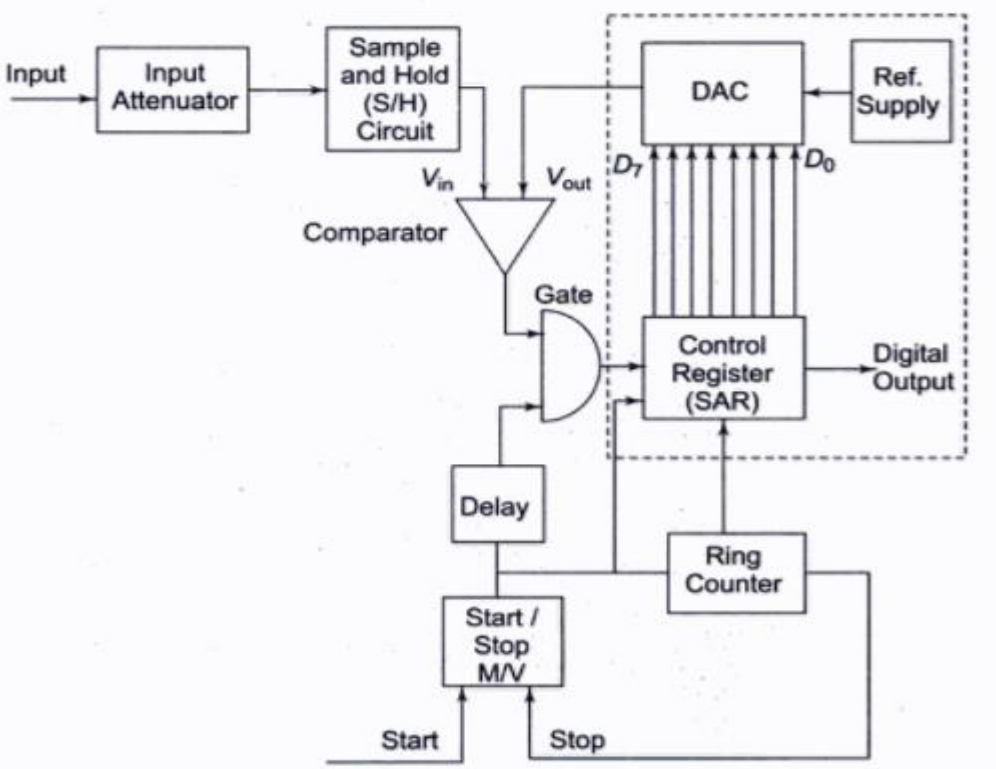


Fig. 2.1 Successive approximation DVM

Suppose if the converter measures a max of 5V and if this corresponds to max count of 11111111. If the test voltage Vin = 1V, the following steps will take place in the measurement.

V_{in} = 1 V	Operation	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Compare	Output	Voltage
00110011	D_7 Set	1	0	0	0	0	0	0	0	$V_{in} < V_{out}$	D_7 Reset	2.5
"	D_6 Set	0	1	0	0	0	0	0	0	$V_{in} < V_{out}$	D_6 Reset	1.25
"	D_5 Set	0	0	1	0	0	0	0	0	$V_{in} > V_{out}$	D_5 Set	0.625
"	D_4 Set	0	0	1	1	0	0	0	0	$V_{in} > V_{out}$	D_4 Set	0.9375
"	D_3 Set	0	0	1	1	1	0	0	0	$V_{in} < V_{out}$	D_3 Reset	0.9375
"	D_2 Set	0	0	1	1	0	1	0	0	$V_{in} < V_{out}$	D_2 Reset	0.9375
"	D_1 Set	0	0	1	1	0	0	1	0	$V_{in} > V_{out}$	D_1 Set	0.97725
"	D_0 Set	0	0	1	1	0	0	1	1	$V_{in} > V_{out}$	D_0 Set	0.99785

Sample and Hold Circuit:

- A sample and hold circuit is shown in Fig 2.3 and it consists of a switch and a capacitor.
- In sample mode, the switch is closed and the capacitor gets charged to the instantaneous value of the input voltage
- In hold mode, the switch is opened and the capacitor holds the voltage that it had at the instant the switch was opened.

- The sample and input and output waveform is shown in Fig. 2.4

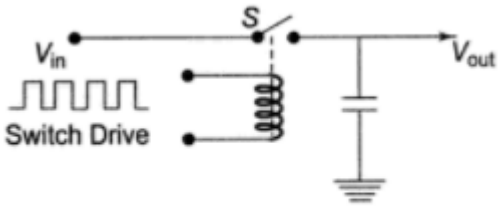


Fig. 2.3 Simple sample hold circuit

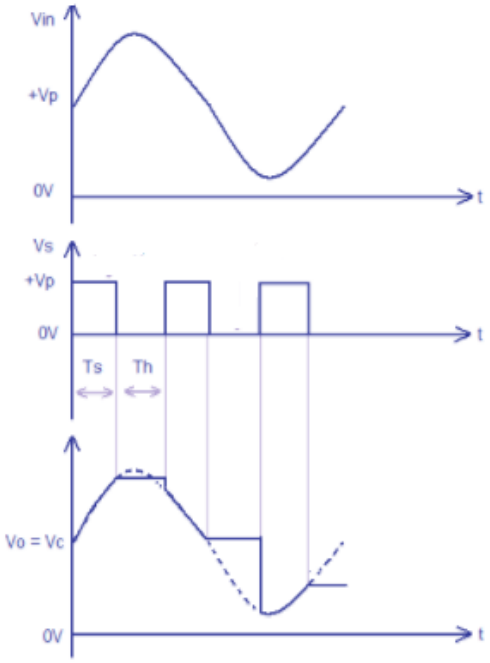


Fig. 2.4. Sample and Hold input and output waveform

Continuous Balance DVM or Servo Balancing Potentiometer Type DVM:

- The block diagram of Continuous Balance Voltmeter is shown in Fig. 2.5.
- It works on the same principle as that of the differential voltmeter or Potentiometric voltmeter.
- The input is a dc signal which is attenuated, overloaded protected and all the ac component is removed and is applied to one input of chopper comparator.
- Chopper is a power switch which converts fixed dc to variable dc and it acts as comparator.The other input to chopper is connected to the variable arm of a precision potentiometer.
- The output of the chopper comparator is driven by the line voltage at the line frequency rate and it is a square wave signal whose amplitude is a function of the difference in voltages connected to the opposite side of the chopper. This is also the error signal
- The square wave signal is amplified and fed to a power amplifier, and the amplified square wave is given to a servomotor which moves the sliding contact of the potentiometer

- The servomotor moves the sliding contact of potentiometer proportional to the error signal.
- When the error signal becomes zero, the servomotor stops moving the sliding contact. Also the servomotor drives a readout.
- When the error signal is zero the readout is proportional to the input.

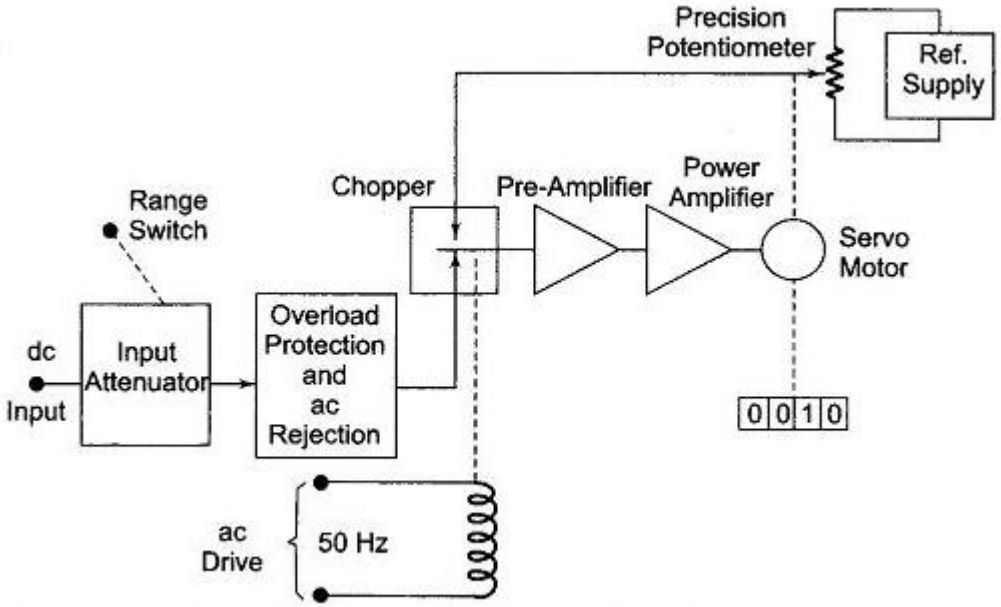


Fig. 2.5 Block Diagram of a Servo Balancing Potentiometer Type DVM

$3\frac{1}{2}$ Digit:

- This is related to the display in the DVM.
- The number of digit positions used in a digital meter determines the resolution. Hence a 3 digit display on a DVM for a 0 –1 V range will indicate values from 000 – 999 mV with a smallest increment of 1 mV. Similarly for 0-10 V range will indicate values from 000 – 9.99V with a smallest increment of 10 mV.
- The fourth digit capable of indicating 0 or 1 (hence called a Half Digit) is placed to the left. This permits the digital meter to read values above 999 up to 1999.
- The 3 ½ digit display is shown in Fig. 2.6

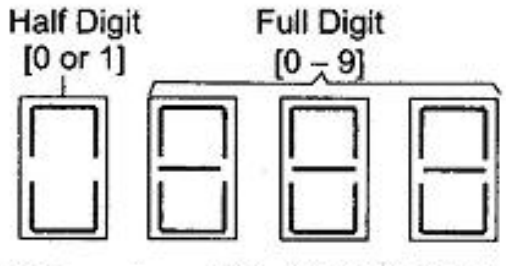


Fig. 2.6 3½–Digit Display

Resolution and Sensitivity of digital meter:

Resolution: Resolution of a DVM is determined by the number of full or active digits used

If n= number of full digits,

then the Resolution (R) $= \frac{1}{10^n}$

If n=3, then the resolution R = $\frac{1}{10^3} = 0.001$

Sensitivity: Sensitivity is the smallest change in input which a digital meter is able to detect. Hence, it is the full scale value of the lowest voltage range multiplied by the meter's resolution.

Sensitivity $S = (fs)_{min} \times R$

Where $(fs)_{min}$ = lowest full scale of the meter

R = Resolution expressed as decimal.

Microprocessor based Ramp type DVM:

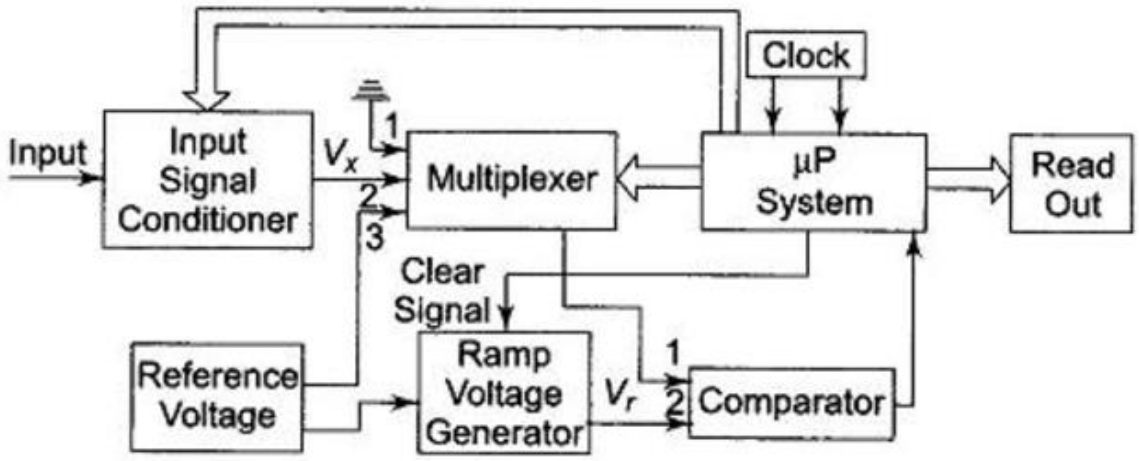


Fig. 2.7 (a) Basic Block Diagram of a Microprocessor-based Ramp Type DVM

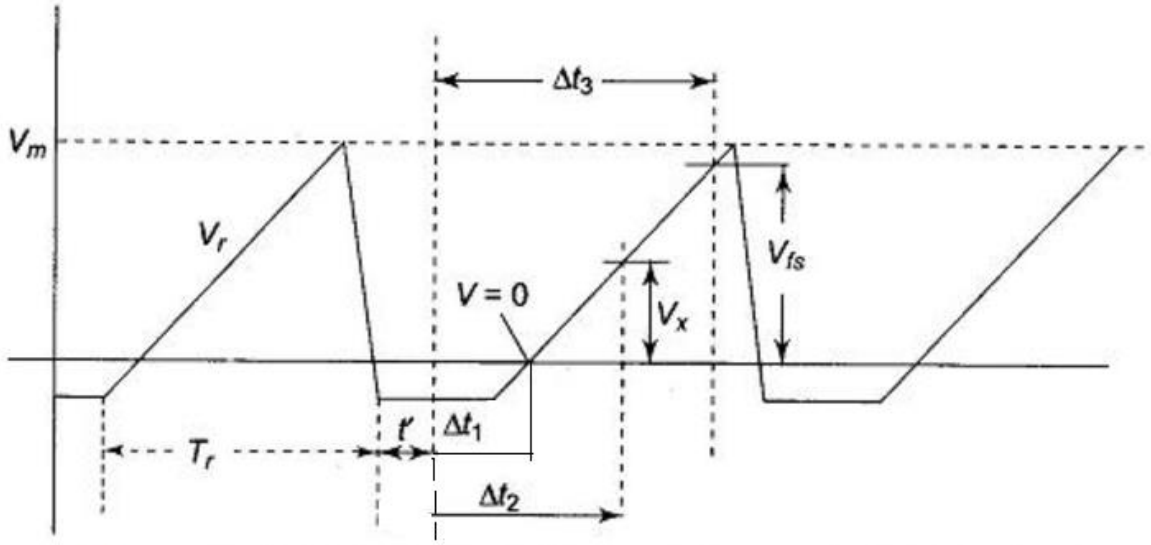


Fig. 2.8 (b) Operating Waveform of a µp-based Ramp Type DVM

- Depending on command fed to control input of multiplexer by microprocessor comparator connects to multiplexer input 1,2,3.
- Input 1 connects to ground, Input 2 connects to unknown input, Input 3 connects to reference voltage input.
- Comparator has two inputs, input 1 accepts output signal from multiplexer and input 2 accepts ramp voltage from ramp generator.
- Microprocessor remain suspended in resting state until it gets start command to start conversion. In this state it regularly send reset signal to ramp generator resets its capacitor discharge producing ramp signal having constant Tr and Vm with with enough time for capacitor discharge.
- When conversion command arrives at time t^1 to microprocessor, multiplexer connects input 1 to comparator input and brings to ground potential i.e zero voltage. Microprocessor pauses until another sawtooth pulse begins.
- Input 2 voltage arrived from ramp generator becomes equal to input 1 and voltage will become zero at time Δt1 and the count during this interval be N1 and it is stored in microprocessor.
- When 2nd command from microprocessor causes comparator input connected to input 2 of multiplexer, i.e: unknown input voltage Vx. In this instant ramp generator voltage will be compared with unknown voltage and Δt2 is the time taken to equal both inputs and number of count during this interval is N2 and it is stored in microprocessor.
- For next command microprocessor causes comparator input connected to input 3 of multiplexer, i.e: reference voltage Vref. In this instant ramp generator voltage will be compared with reference voltage and Δt3 is the time taken to equal both inputs and number of count during this interval is N3 and it is stored in microprocessor.
- Then microprocessor computes unknown voltage Vx by

$$Vx = C.\frac{(N2-N1)}{(N3-N1)}$$

Where C is coefficient dependent characteristic of the instrument.
N1,N2,N3 are the counts represents zero drift, unknown voltage and full scale voltage.

Advantages:

- Its scale size remains constant due to zero drift correction and maximum
- The accuracy of the instrument is not affected by the time and temperature instabilities of the circuit element values.
- There is a good repeatability in switching instants in the presence of noise and interference. This is because the ramp approaches the point at which the comparator operates always the same side and always the same rate.

Disadvantages

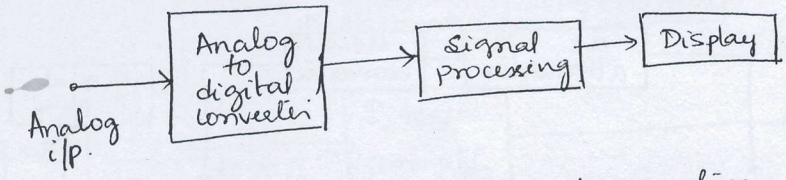
- Noise and interference cannot be suppressed.

General Specifications of DVM:

Display	:	3-1/2 digits, LCD
Unit Annunciation	:	mV, V, mA, Ω, kΩ, MΩ, buzzer, B(low battery)
	:	MANU (Manual), ac and ⊣▷⊢ (diode test)
Max. Indication	:	1999 or – 1999
Over-range indication	:	only (1) or (– 1) displayed at the MSB position.
Polarity	:	AUTO negative polarity indication.
Zero adjustment	:	Automatic
Functions	:	DC volts, AC volts, DC amps, AC amps, Ohms, continuity test, diode test.
Ranging	:	Selectable automatic or manual
Automatic	:	Instrument automatically selects maximum range for measurement and display. Auto ranging operates on all functions except for dc or ac current.
Manual	:	Switch selection as desired
Sampling Rate	:	2 sample/s, nominal
Low Battery	:	B mark on LCD readout
Temperature	:	Operating 0°C – 40°C, < 80% RH (Relative humidity)
	:	Storage – 20°C – 60°C, < 70% RH
Power	:	Two AA size 1.5 V batteries. Life 2000 hours typically with zinc-carbon.
Standard accessories	:	Probe red-black, safety fuse 250 – 0.2 A
Size	:	160 (L) × 80 (B) × 30 (H)
Weight	:	250 g without batteries.
Input impedance	:	11 MΩ – 1000 MΩ
Accuracy	:	± 0.5% – 0.7% or ± 5 digit for dc
	:	1.0% reading or ± 5 digit for ac at 40 – 500 kHz

Digital Instruments

* The analog measuring instruments are being replaced b the digital instruments.
* A digital measuring instrument can measure volta current, power, frequency and logic.
* The block diagram of digital instrument is



* Thus in a digital instrument system it has a convert at the i/p stage.
* The display can be analog or digital in nature.
  - → If analog readout — It needs a Digital to ana convertor and deflection area
  - → If digital readout — with some signal processing data can be readout direct
* In general a digital system may include Resistors, Capacitors, Transistors, Linear IC's, Digital Display devices, ADC & DAC (convertor).

Digital Multimeter:-

Digital meters have the following advantages.

- → High accuracy
- → High input impedance
- → smaller in size
- → gives unambiguous reading
- → O/p is available such that it can be interfaced with devices also can be readout.

Analog meters have the following advantages.

- → They do not need power supply.
- → Better visual indication of sudden changes in the parameter.

DIGITAL MULTIMETER

- A digital multimeter is used to measure voltage, current and resistance.
- A DMM is made up of several A/D converters, circuitry for counting and attenuation circuit.
- To measure resistance-the unknown resistor is connected across the input probes. Some current flows through the resistor, from constant current source.
- Now according to ohm's law voltage is produced across it which is directly proportional to its resistance, then fed to A/D converter, to get the digital display.
- To measure AC voltage-connect an unknown AC voltage across input probes. The voltage is attenuated, if it is above the selected range and then rectified to convert it into proportional DC voltage. It then fed to A/D converter, to get the digital display.
- To measure DC voltage-connect an unknown DC voltage across input probes. The voltage is attenuated, if it is above the selected range and then directly fed to A/D converter, to get the digital display.
- To measure AC current-connect an unknown AC current across input probes. The current is converted proportionally into voltage with help of current to voltage converter and then rectified. Now the voltage in terms of AC current is fed to A/D converter, to get the digital display.
- To measure DC current--connect an unknown DC current across input probes. The current is converted proportionally into voltage with help of current to voltage converter and then rectified. Now the voltage in terms of DC current is fed to A/D converter, to get the digital display.

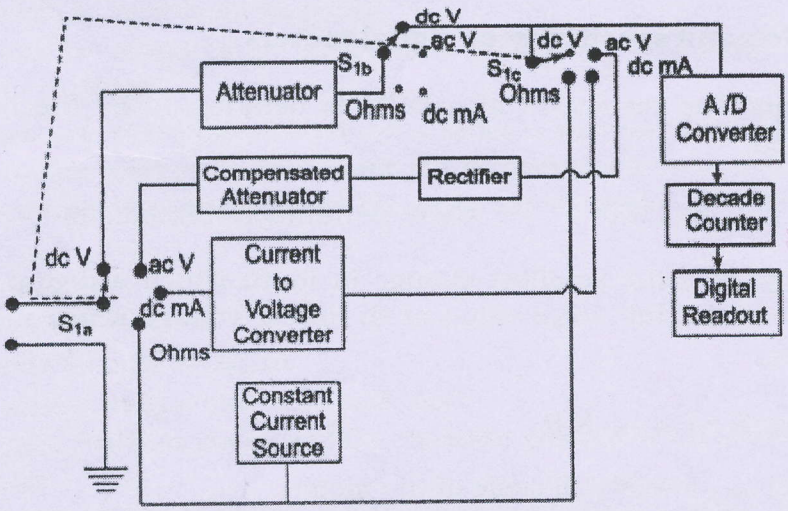


Fig: Block diagram of Basic Digital Multi-meter

- Current to voltage converter- The current to be measured is applied to the summing junction ($\sum i$) at the input of the opamp.
  Since the opamp has very high input impedance, the current I_R is very nearly equal to I_i. The current I_R causes a voltage drop which is proportional to current, to be developed across the resistor.
  This voltage drop is the input to A/D converter, thereby providing a reading that is proportional to the unknown current.

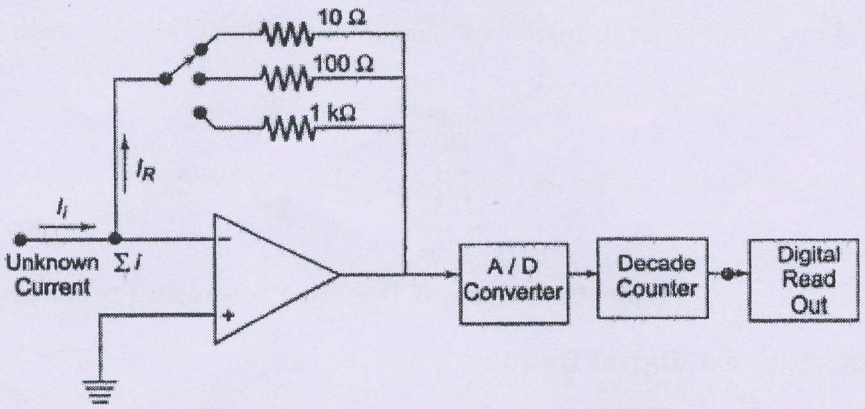


Fig: current to voltage converter

The basic circuit shown below is always a dc voltmeter

- Current is converted to voltage by passing it through a precision low shunt resistance, while ac current is converted into dc by employing rectifiers and filter circuits.
- For resistance measurement, the meter includes a precision low current source that is applied across the unknown resistance, which gives a dc voltage which is digitized and readout as ohms.

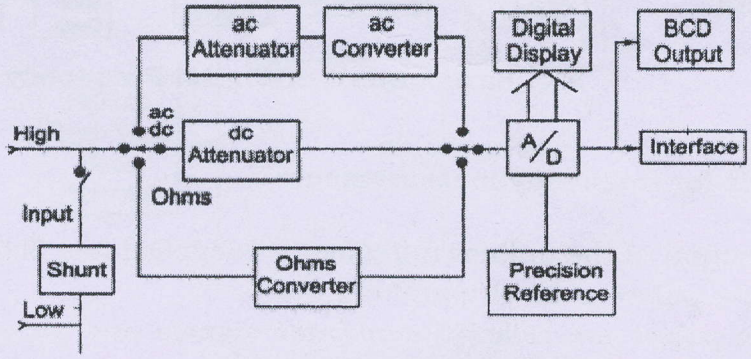


Fig: Digital multi-meter

DIGITAL FREQUENCY METER

Principle of operation

- The signal whose frequency is to be measured is converted into a train of pulses, one pulse for each cycle of the signal.
- The number of pulses occurring in a definite interval of time is counted by electronic counter.
- The number of counts is direct indication of the frequency of the signal (unknown).

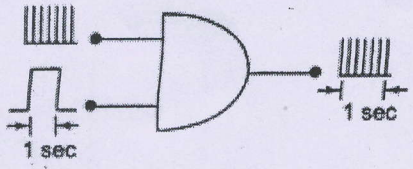


Fig: Principle of Digital Frequency measurement

Basic circuit of a digital frequency meter

- The signal is amplified before applying it to Schmitt trigger.
- The Schmitt trigger converts the input signal into square wave which then differentiated and clipped to obtain train of pulses, one pulse per each cycle of signal.
- The outputs from Schmitt trigger are fed to START/STOP gate.
- When this gate is enabled, the input pulses pass through this gate and are fed directly to electronic counter, which counts the number of pulses.
- When this gate is disabled, the counter stops counting the incoming pulses.

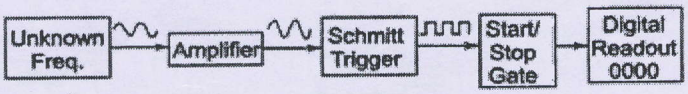


Fig: Basic circuit of Digital Frequency meter

Basic circuit for frequency measurement

- The output of the unknown frequency is applied to a Schmitt trigger, producing positive pulses at its output.
- These pulses are called the **counter signals** and present at point A of main gate.
- Positive pulses from the time base selector are present at point B of START gate and point B of the STOP gate.
- Initially the flip flop (F/F-1) is at logic 1 state. The resulting voltage from output Y is applied to point A of the STOP gate and enables this gate. The logic 0 stage

at the output $\overline{Y}$ of the F/F-1 is applied to the input A of the START gate and disables the gate.

- As the STOP gate is enabled, the positive pulses from the time base pass through the STOP gate to the Set(S) input of the F/F-2 thereby setting F/F-2 to state 1.
- The resulting 0 output level from $\overline{Y}$ of F/F-2 is applied to terminal B of the main gate.
- In order to start the operation, a positive pulse is applied to reset input of F/F-1, thereby causing its state to change.
- Hence Y=1, Y=0, and as a result the STOP gate is disabled and the START gate enabled.
- This read pulse is simultaneously applied to reset the counters, so that counting can start.
- When the next pulse from the time base arrives, it is able to pass through the START gate to reset F/F-2, therefore the F/F-2 output changes state from 0 to 1, hence $\overline{Y}$ changes from 0 to 1.
- This resulting positive voltage from $\overline{Y}$ called the **gating signal** is applied to input B of the main gate thereby enabling the gate.
- Now the pulses from the unknown frequency source pass through the main gate to the counter and the counter start counting. This same pulse from the START gate is applied to set input of F/F-1,changing its state from 0 to 1
- This disables the START gate enables the STOP gate.

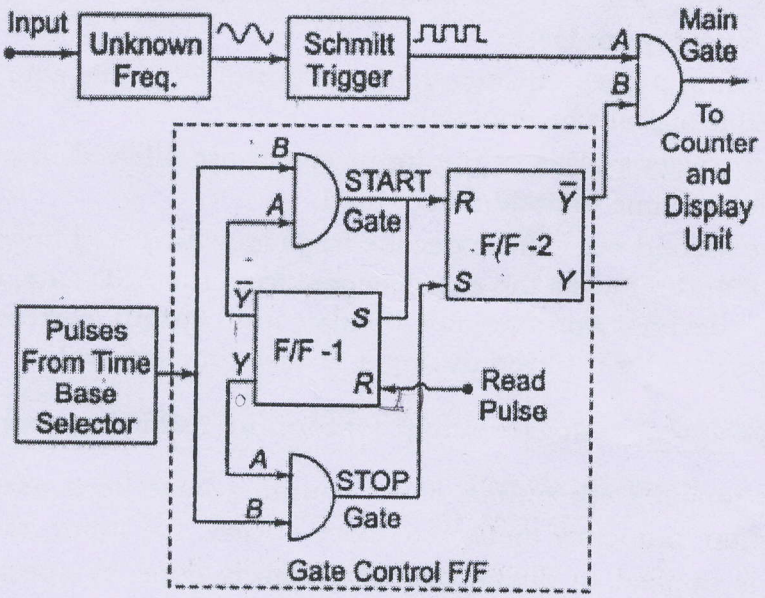


Fig: Basic circuit for measurement of frequency showing gate control F/F

Block diagram of a digital frequency meter

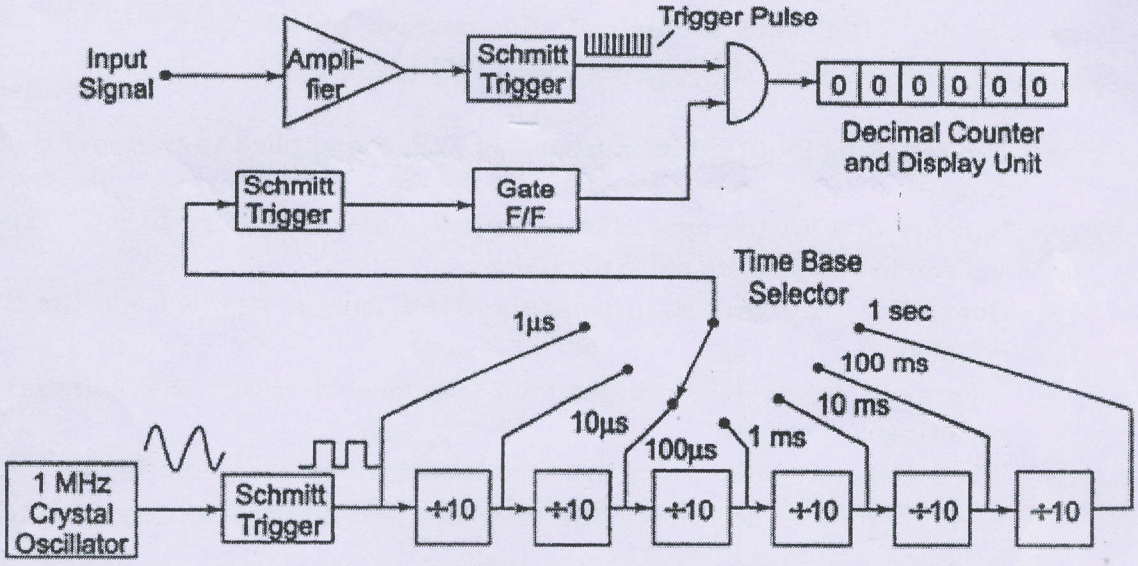


Fig: Block diagram of a digital frequency meter

- The input signal is amplified and converted to a square wave by a Schmitt trigger circuit, which is then differentiated and clipped to produce a train of pulses, each separated by the period of the input signal.
- The time base selector output is obtained from the oscillator and is converted into positive pulses.
- The first pulse activates the gate control F/F. this gate control F/F provides the enable signal t he and gate.
- The trigger pulses of the input signal are allowed to pass through the gate for selected time period and counted.
- The second pulse from decade frequency divider changes the state of the control F/F and removes the enable signal from the AND gate, thereby closing it.
- The decimal counter and display unit output corresponds to the number of input pulses received during a precise time interval.

High Frequency Measurement (extending frequency range)

- Techniques other than direct counting have been used to extend the range of digital frequency meters to above 40GHz .the input frequency is reduced before it is applied to digital counter. This is done by special techniques. Some are follows
    1. **Prescaling**: The high frequency signal by the use if high speed is divided by the integral numbers such as 2,4,6,8 etc. divider circuits, to get it within the frequency range of DFM.

2. **Heterodyne converter**: The high frequency signal is reduced in frequency to range within that of the meter, by using heterodyne techniques.
3. **Transfer oscillator**: A harmonic or tunable LF continuous wave oscillator is zero beat with the unknown high frequency signal. The LF oscillator frequency is measured and multiplied by an integer which is equal to the ratio of two frequencies, in order to determine the value of unknown HF.
4. **Automatic Divider**: The high frequency signal is reduced by some factor, such as 100:1, using automatically tuned circuits which generated an output frequency equal to $1/100^{th}$ or $1/1000^{th}$ of the input frequency.

DIGITAL MEASUREMENT OF TIME

Time Base Selector

- The time base selector consists of a fixed frequency crystal oscillator, called the clock oscillator.
- The output of clock oscillator is fed to Schmitt trigger, which converts the input sine wave to output consisting of train pulses at the rate equal to the frequency of clock oscillator.
- The train of pulses is then passed through a series frequency divider decade assemblies connected in cascade.
- Each decade divider consists of a decade counter and divides the frequency by ten.
- Outputs are taken from decade frequency divider by means of selector switch.

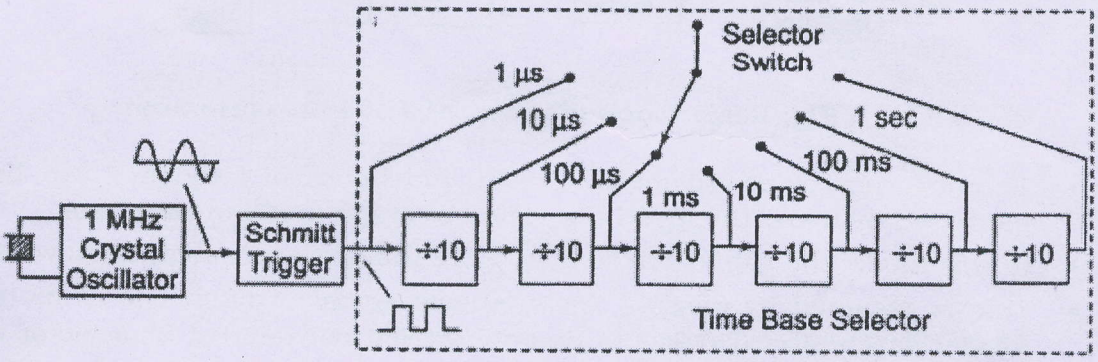


Fig: Time Base Selector

Measurement of time (period measurement)

Principle of operation

- The beginning of time period is start pulse originating from input 1 and end of time period is stop pulse coming from input 2.
- The oscillator runs continuously, but oscillator pulses reach the output only during the period when the control F/F is in 1 state.
- The number of pulses counted is a measure of time period.

Block diagram explanation:

- The gating signal is derived from the unknown input signal, which controls the enabling and disabling of the main gate.
- The number of pulses which occur during one period of the unknown signal are counted and displayed by the decade counting assemblies.
- The only disadvantage is that the operator has to calculate the frequency from time by using the equation f=1/T.

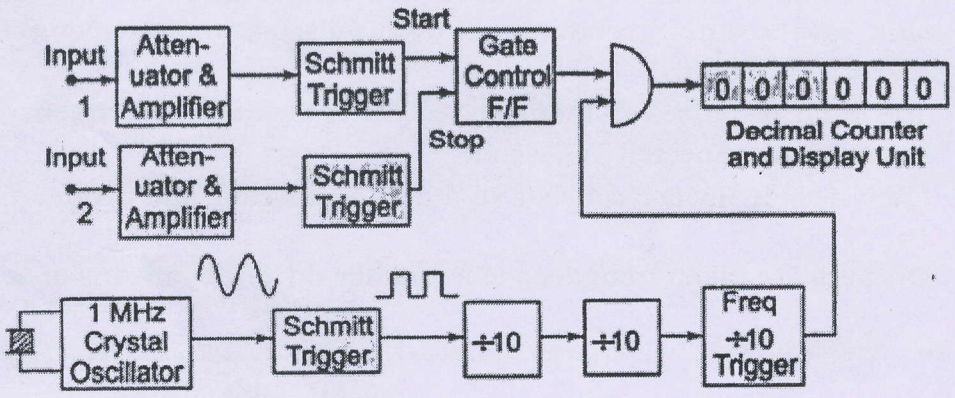


Fig: Basic block diagram of Time measurement

- The accuracy of period measurement and hence of frequency can be greatly increased by using the **multiple period average mode** of operation.
- In this mode, the gate is enabled for more than one period of unknown signal.
- This is obtained by passing the unknown signal through one or more decade divider assemblies (DDAs), so that the period is extended by a factor of 10000 or more.
- The decimal point location and the measurement units are changed when each time an additional decade divider is added, so that the display is always in terms of the period of one cycle of input signal.

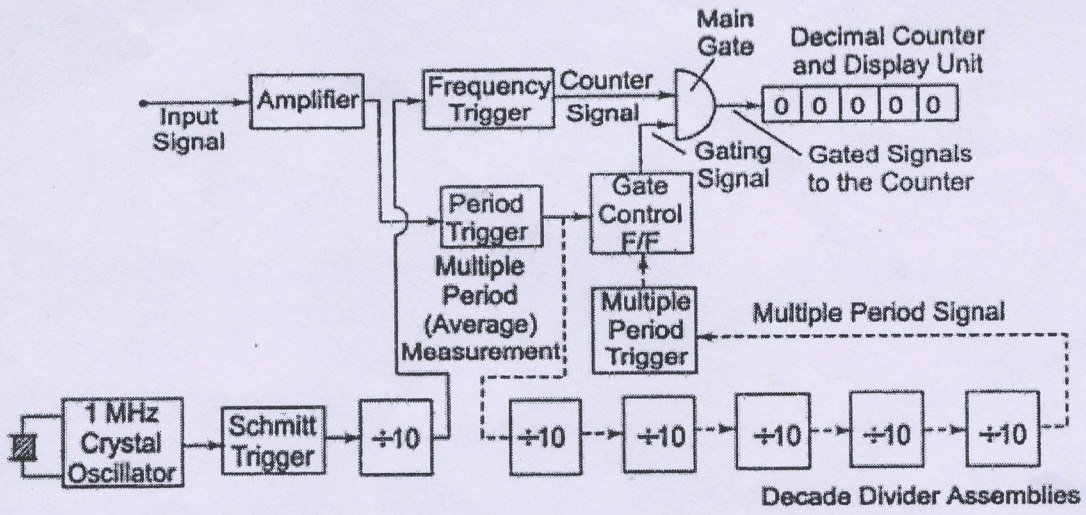


Fig: Block diagram of a single and multiple periods (average) measurement

Ratio and multiple ratio measurement

- The ratio measurement involves the measurement of the ratio of two frequencies.
- A low frequency is used as gating signal while high frequency is the counted signal.
- The number of cycles of high frequency signal which occurs during the period of lower frequency signal are counted and displayed by the decimal counter and display unit.
- In multiple ratio measurements the period of low frequency signal is extended by a factor of 10, 100 etc by using DDAs.

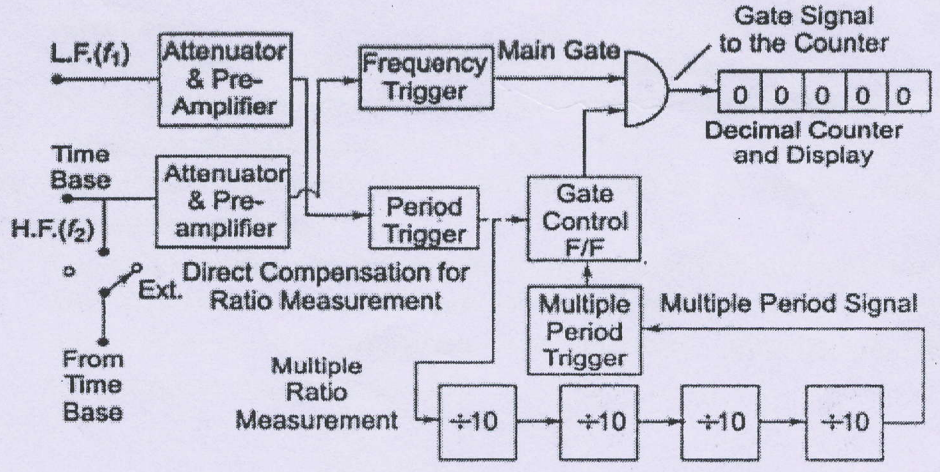


Fig: Block diagram for Ratio and multiple ratio measurement

NOTE: For staircase RAMP ADC refer other class notes or text book

Universal Counter :-

→ Universal counter can be considered as a block which can do all measure measurements of time ~~period~~ period & freq in the same ckt.

→ It is the combinations of various circuits (like time freq, ratio measurements etc) which is assembled together to form one complete block known as 'Universal Counter Timer'.

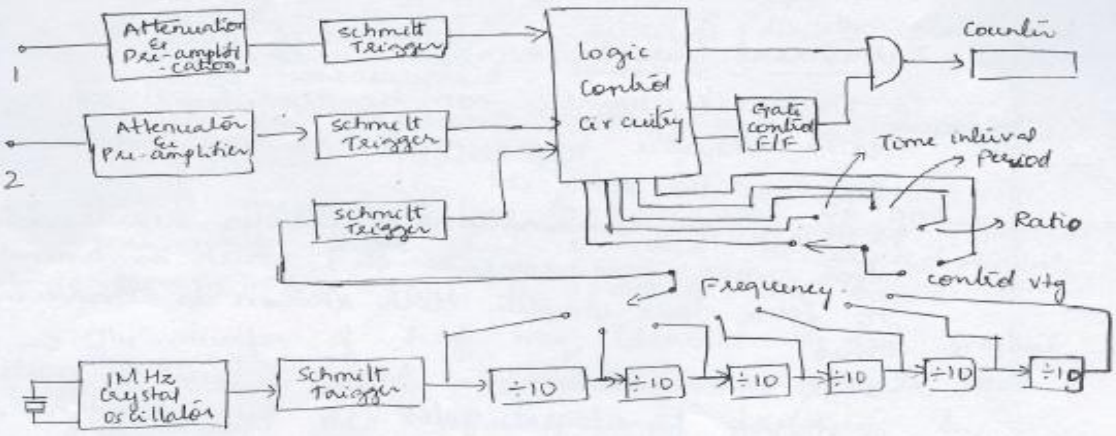
→ The universal counter has a 'function switch' which is driven by logic gates & this switch controls and selects the function of universal counter

→ When the function switch is in the frequency mode, the signal whose freq is to be measured is connected to counter signal of the main gate simultaneously from the time base selector proper time is selected & provided through gate control F/F which enables & disables the main gate. Both the paths are connected / latched so that they operate in proper sequence. All the controlling is done by the logic circuitry.

→ When the function switch is connected to period measurement mode, the logic circuitry connects the unknown signal for enabling & disabling the main gate. Simultaneously connects the signal from time base selector to the counter signal of the main gate.

→ Similarly when the function switch is in other position it performs different functions like ratio, multiple ratio measurement ~~ect~~ etc.

→ The main part is the logic ckty in universal counter



Digital Tachometer:

- A digital Tachometer is digital device which measure the speed of a rotating object. A rotating object can be a ceiling fan, motor shaft, car tire etc. The block diagram is shown in Fig. a
- The technique employed for measurement is similar to the technique used in a conventional frequency counter, except that the selection of the gate period is in accordance with the rpm calibration.
- If we consider R as the rpm of a rotating shaft.
- Let P be the number of pulses produced by the pick-up for one revolution of the shaft, now if this is divided by 60 it gives number of no. of pulses per minute as P/60.
- Therefore, in one minute the number of pulses from the pick-up will be R × P/60.
- Now if G is the gating period, and the pulses counted within the gating period will be given by
    - (R × P × G)/60
- This can be calibrated to get direct reading by selecting G as 60/P

Then this will result in

$$\frac{R \times P \times 60}{60 \times P} = R$$

Thus the relation between gate period and no. of pulses is G = 60/P and if G is fixed for 1s (G=1s) then revolution pick up must be capable of producing 60 pulses per revolution.

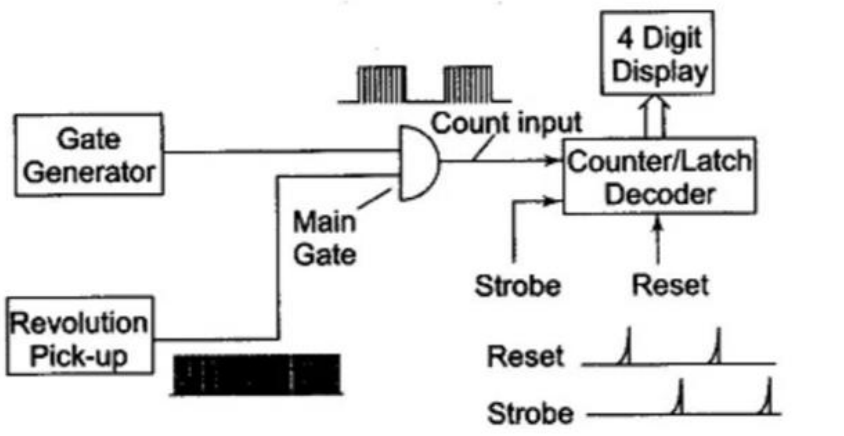


Fig. a Basic Block Diagram of a Digital Tachometer

Digital pH meter:

- A pH meter is an instrument whuch measures the hydrogen-ion activity in water-based solutions, indicating its acidity or alkalinity expressed as pH. The output of pH meter is the difference in electrical potential between a pH electrode and a reference electrode.
- pH is a quantative measure of acidity. If the pH is less than 7, the solution is acidic (the lower the pH, the greater the acidity). A neutral solution has a pH of 7 and alkaline (basic) solutions have a pH greater than 7.

The pH unit is defined as

$$pH = - \log (\text{concentration of } H^+)$$

Where H^+ is the hydrogen or hydronium ion.

- The basic block diagram of a digital pH meter is shown in Fig. b
- A digital pH meter differs from an ordinary pH meter, where the meter has an analog to digital converter (ADC) and a digital display. The ADC used for this application is the dual slope converter.
- The dual slope ADC generates a pulse which has a duration proportional to the input signal voltage (T pulse width signal). This pulse width is converted to a digital signal using the signal from oscillator (which generates a count digital signal). The count signal is counted and displayed.

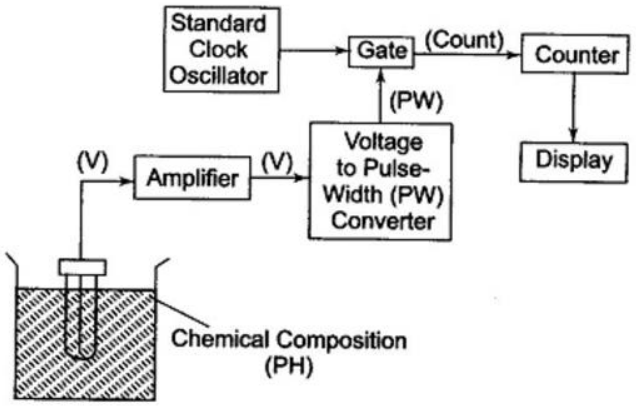


Fig. b Digital pH Meter

Digital Phase meter:

- A phase meter measures the phase difference between 2 signals of same frequencies.
- The block diagram consists of two pairs of preamplifier's for conditioning the input signal, zero crossing detectors to shape the input signal to a square waveform without any change in their phase, J-K F/Fs, and a single control gate.
- The process of measuring the phase difference is illustrated by the schematic diagram shown in Fig. c.
- Two signals having phases Po and Px respectively are applied as inputs to the preamplifier and attenuation circuit. The frequency of the two inputs should be same and their phases are different.
- As input Po signal increases in the positive half cycle, the ZCD detects the change in state when the input crosses zero (0) giving a high (1) level at the output. This causes the J-K F/F-1's output (Q) to go high.
- This high output from the F/F-1 enables the AND gate, and pulses from the clock are fed directly to the counter. The counter starts counting these pulses.
- Also this high output level of F/F-1 is applied to the clear input of J-K F/F-2 which clears the output of the F/F-2 (i.e Q of F/F-2 is 0).

- Now as the other input Px which has a phase difference with respect to Po, crosses zero in positive half cycle, the ZCD detects and causes its output to go high (1). This high input is given to J-K F/F-2, causing its output go high.

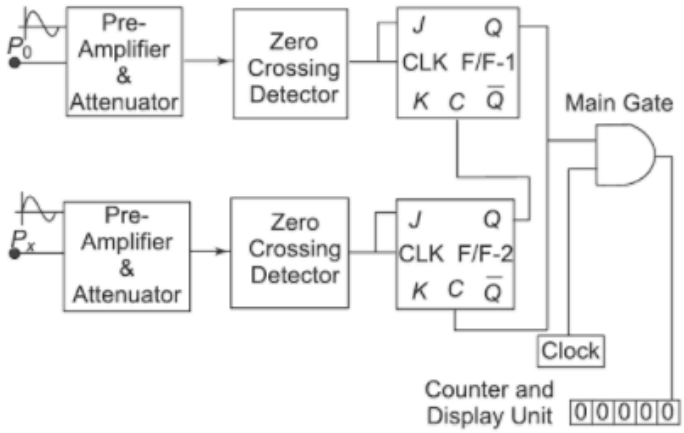


Fig. c Digital phase meter

- This high output (Q) of F/F-2 is connected to the clear input of F/F-1 forcing the F/F-1 to clear/reset and its output goes to 0.
- The AND gate is thus disabled, and the counter stops counting.
- The number of pulses counted while enabling and disabling the AND gate is in direct proportion to the phase difference, hence the display unit gives a direct readout of the phase difference between the two inputs having the same frequency.

Digital Capacitance Meter:

The principle of operation involves counting the no. of pulses derived from constant frequency oscillator during a fixed interval produced by another lower frequency oscillator. This oscillator uses the capacitor being measured as the timing. The capacitance measurement is proportional to the counting during fixed time interval.

- Since the capacitance is linearly proportional to the time constant i.e,
  - $\tau = RC$
- Thus the capacitor is charged by a constant current source and discharged through a fixed resistance. The 555 timer along with some digital test equipment is used to measure capacitances. This method is illustrated in Fig. d.
- By choosing the right size of charging resistance, can get a reading directly in microfarads or nanofarads. This measurement method easily measures electrolytic type up to the tens of thousands of microfarads.
- A better way is to measure only the capacitor discharge time.
- In the circuit, the 555 timer is used as an astable multivibrator. When the capacitor charges to its max i.e at the peak of the charging curve, a digital counter is reset, the **gate** is enabled and a clock of 100 kHz pulses is turned on.
- As the gate is enabled the counter starts counting till the discharge portion of the cycle is completed.
- As the capacitor discharges completely, the input to the **gate** is disabled and counter stops counting and the display is updated and the value of the capacitor is readout.

- By selecting the proper reference frequency and charging currents, one can obtain a direct digital display of the value of the capacitance.
- But precaution should be taken to make sure to properly shield the leads and keep them short for low capacity measurements, since the 50 Hz hum can cause some slight instability.

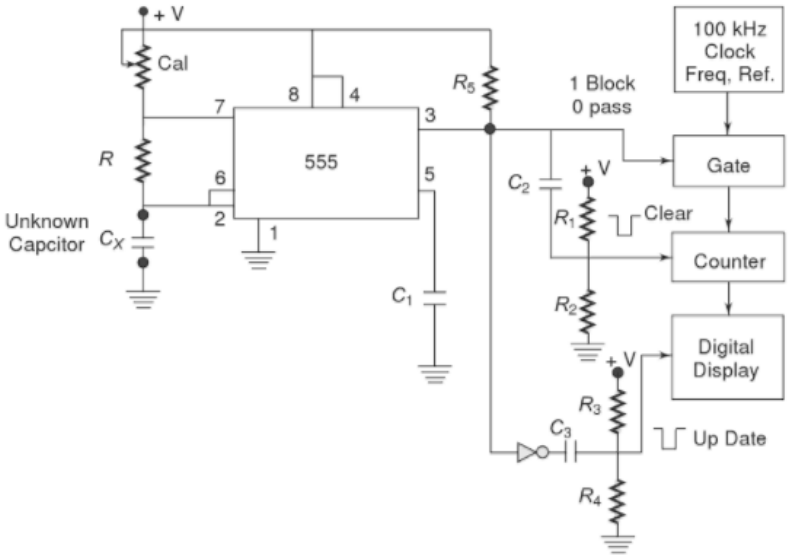


Fig. d Block diagram of a basic digital capacitance meter

Microprocessor based instrument:

The digital instruments are designed and constructed with logic circuits without memory but with the use of microprocessor in measuring instrument, it is considered as a new class of instruments called intelligent instruments.

Fig. e shows the block diagram of microprocessor based

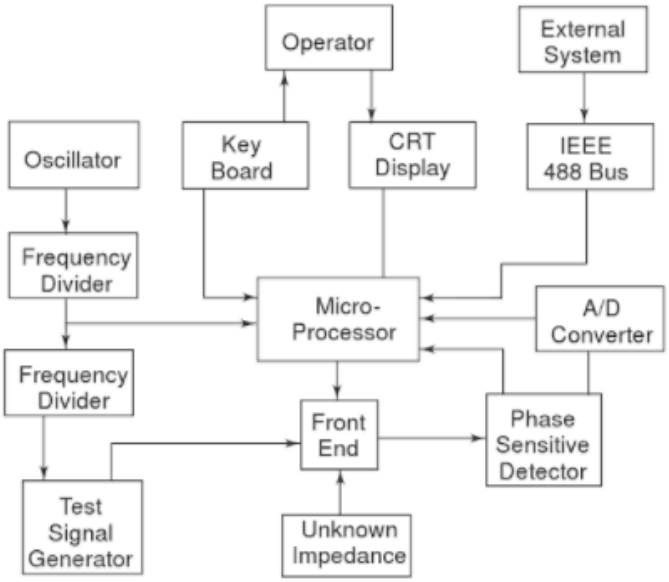


Fig. e Block diagram of a μp (microprocessor) based instrument

- The front end provides the test signal for unknown impedance under measurement and a standard impedance.
- This produces a voltage drop with phase shift proportional to the voltage across it.
- The phase sensitive detector detects this and converts the ac input of impedance in vector form to a dc output.
- This dc input is provided to ADC which gives the digital data which is used by the microprocessor to compute the unknown value of the impedance.
- This value is displayed on the CRT or can be sent as output to the IEEE 488 bus (used to provide interface between instruments)