MODULE-2

POWER TRANSISTORS

Structure

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2.0 Introduction

Power transistors are devices that have controlled turn-on and turn-off characteristics. These devices are used a switching devices and are operated in the saturation region resulting in low on-state voltage drop. They are turned on when a current signal is given to base or control terminal. The transistor remains on so long as the control signal is present.

Power transistors are classified as follows

- Bipolar junction transistors(BJTs)
- Metal-oxide semiconductor filed-effect transistors(MOSFETs)
- Static Induction transistors(SITs)
- Insulated-gate bipolar transistors(IGBTs)

2.1 Objectives:

- To explain different power transistors, their steady state and switching characteristics and limitations.

2.2 Bipolar Junction Transistors

The need for a large blocking voltage in the off state and a high current carrying capability in the on state means that a power BJT must have substantially different structure than its small signal equivalent. The modified structure leads to significant differences in the I-V characteristics and switching behavior between power transistors and its logic level counterpart.

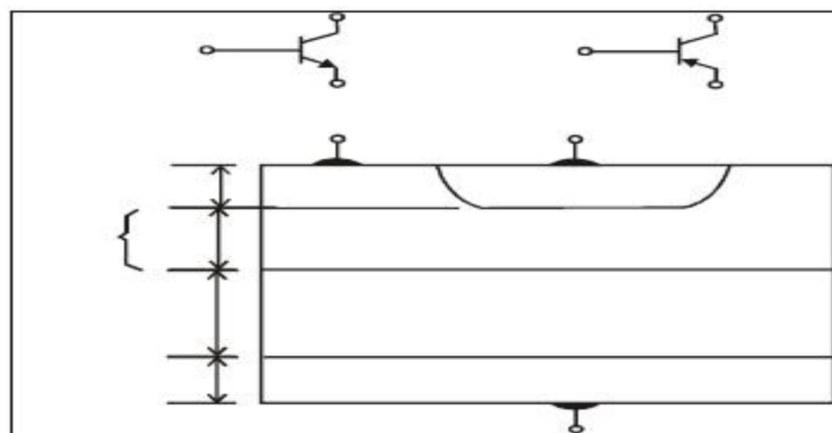
Basic Operating Principle of a Bipolar Junction Transistor

A junction transistor consists of a semiconductor crystal in which a p type region is sandwiched between two n type regions. This is called an n-p-n transistor. Alternatively an n type region may be placed in between two p type regions to give a p-n-p transistor. Fig shows the circuit symbols and schematic representations of an n-p-n and a p-n-p transistor. The terminals of a transistor are called Emitter (E), Base (B) & Collector (C) as shown in the figure.

When a biasing voltage VBB of appropriate polarity is applied across the junction JBE the potential barrier at this junction reduces and at one point the junction becomes forward biased. The current crossing this junction is governed by the forward biased p-n junction equation for a given collector emitter voltage. The base current iB is related to the recombination of minority carriers injected into the base from the emitter. The rate of recombination is directly proportional to the amount of excess minority carrier stored in the base. Since, in a normal transistor the emitter is much more heavily doped compared to the base the current crossing J B BE is almost entirely determined by the excess minority carrier distribution in the base. Thus, it can be concluded that the relationship between iBB and VBE will be similar to the i-v characteristics of a p-n junction diode. VCE, however have some effect on this characteristic. As VCE increases reverse bias of JCB increases and the depletion region at JCB moves deeper into the base. The effective base width thus reduces, reducing the rate of recombination in the base region and hence the base current. Therefore iB for a given V B BE reduces with increasing VCE

Power Transistor Structure

If we recall the structure of conventional transistor we see a thin p-layer is sandwiched between two n-layers or vice versa to form a three terminal device with the terminals named as Emitter, Base and Collector. The structure of a power transistor is as shown below.



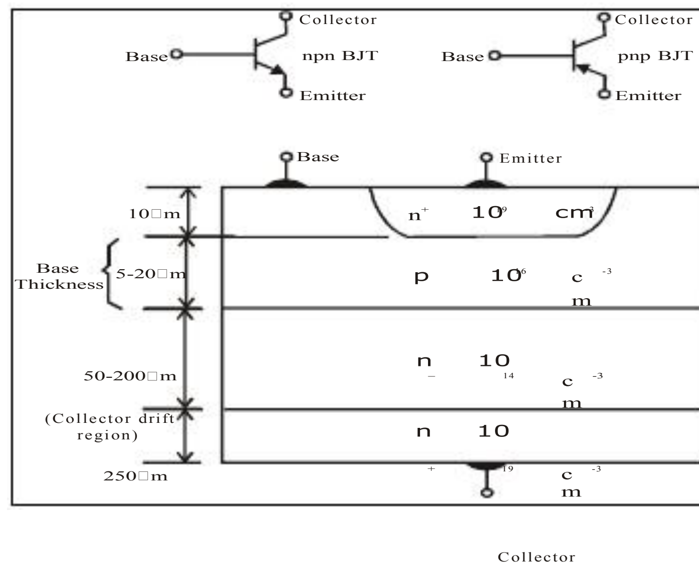


Fig.2.1: Structure of Power Transistor

The difference in the two structures is obvious.

A power transistor is a vertically oriented four layer structure of alternating p-type and n-type. The vertical structure is preferred because it maximizes the cross sectional area and through which the current in the device is flowing. This also minimizes on-state resistance and thus power dissipation in the transistor.

The doping of emitter layer and collector layer is quite large typically 10^{19} cm^{-3}. A special layer called the collector drift region (n^-) has a light doping level of 10^{14}.

The thickness of the drift region determines the breakdown voltage of the transistor. The base thickness is made as small as possible in order to have good amplification capabilities, however if the base thickness is small the breakdown voltage capability of the transistor is compromised.

Steady State Characteristics

Figure 3(a) shows the circuit to obtain the steady state characteristics. Fig 3(b) shows the input characteristics of the transistor which is a plot of I_B versus V_{BE} . Fig 3(c) shows the output characteristics of the transistor which is a plot I_C versus V_{CE} . The characteristics shown are that for a signal level transistor.

The power transistor has steady state characteristics almost similar to signal level transistors except that the V-I characteristics has a region of quasi saturation as shown by figure 4.

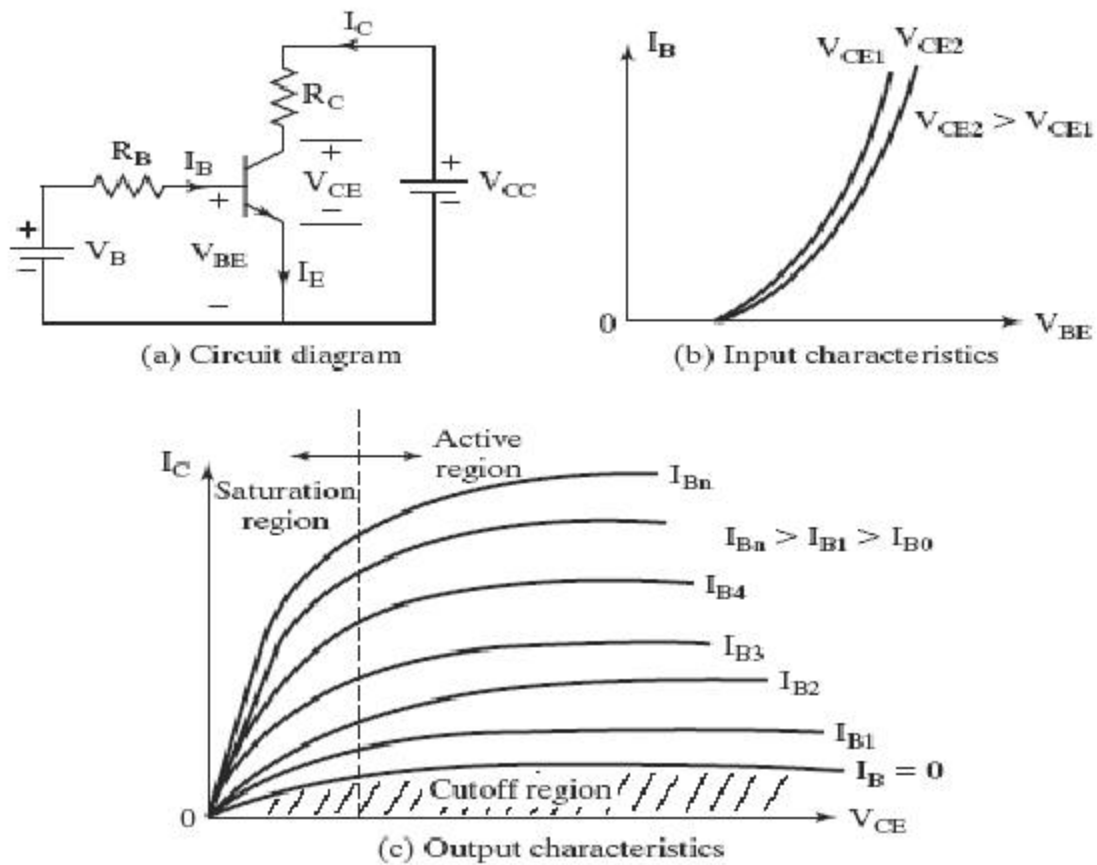


Fig 2.2. Steady State Characteristics of Power Transistor

There are four regions clearly shown: Cutoff region, Active region, quasi saturation and hard saturation. The cutoff region is the area where base current is almost zero. Hence no collector current flows and transistor is off. In the quasi saturation and hard saturation, the base drive is applied and transistor is said to be on. Hence collector current flows depending upon the load.

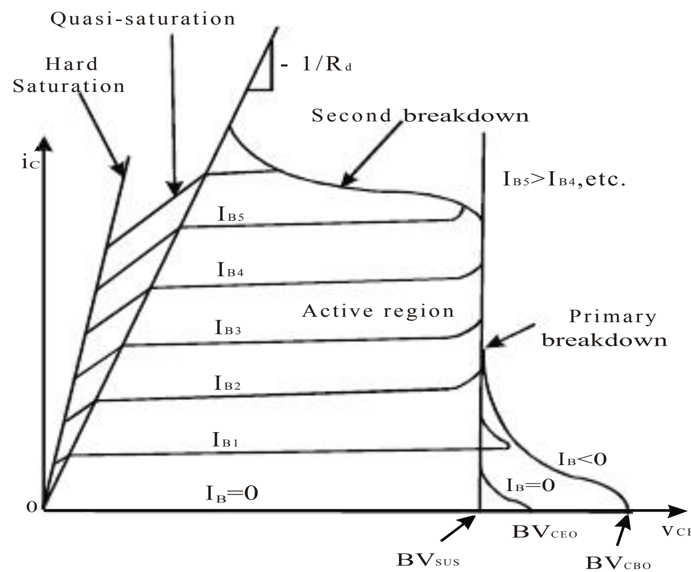


Fig. 2.3: Characteristics of NPN Power Transistors

The power BJT is never operated in the active region (i.e. as an amplifier) it is always operated between cutoff and saturation. The BV_{SUS} is the maximum collector to emitter voltage that can be sustained when BJT is carrying substantial collector current. The BV_{CEO} is the maximum collector to emitter breakdown voltage that can be sustained when base current is zero and BV_{CBO} is the collector base breakdown voltage when the emitter is open circuited.

The primary breakdown shown takes place because of avalanche breakdown of collector base junction. Large power dissipation normally leads to primary breakdown.

The second breakdown shown is due to localized thermal runaway.

Transfer Characteristics

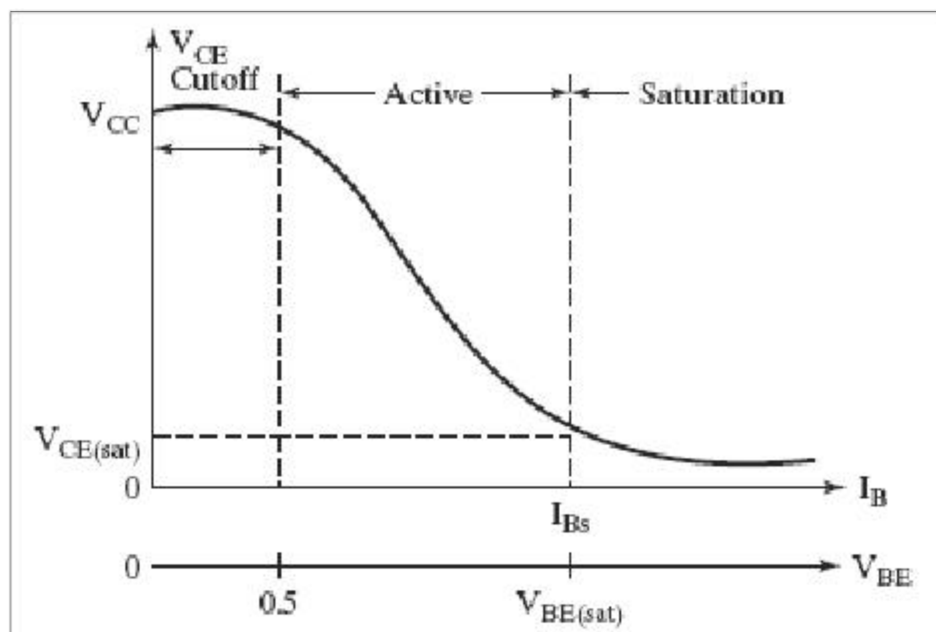


Fig. 2.4: Transfer Characteristics

B

$$I_E = I_C + I_B$$

$$\beta = h_{fE} = \frac{I_C}{I_B}$$

$$I_C = \beta I_B + I_{CEO}$$

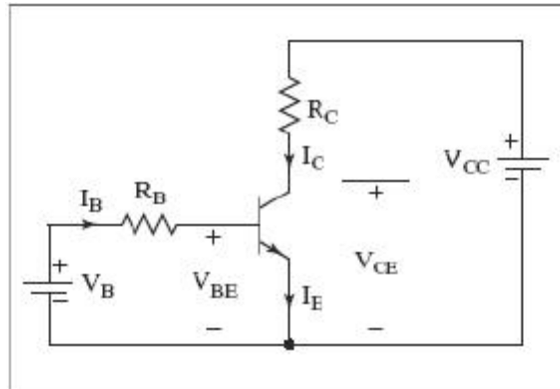
$$\alpha = \frac{\beta}{\beta + 1}$$

$$\beta = \frac{\alpha}{1 - \alpha}$$

2.3 Transistor as a Switch

The transistor is used as a switch therefore it is used only between saturation and cutoff.

From fig. 5 we can write the following equations



\Fig. 2.5: Transistor Switch

$$I_B = \frac{V_B - V_{BE}}{R_B}$$

$$V_C = V_{CE} = V_{CC} - I_C R_C$$

$$V_C = V_{CC} - \beta \frac{R_C \;\; V_B - V_{BE}}{R_B}$$

$$V_{CE} = V_{CB} + V_{BE}$$

$$V_{CB} = V_{CE} - V_{BE} \qquad \ldots.$$

Equation (1) shows that as long as V_{CE} □ V_{BE} the CBJ is reverse biased and transistor is in active region, The maximum collector current in the active region, which can be obtained by setting V_{CB} □ 0 and V_{BE} □ V_{CE} is given as

$$I_{CM} = \frac{V_{CC} - V_{CE}}{R_C} \qquad \therefore \qquad I_{BM} = \frac{I_{CM}}{\beta_F}$$

If the base current is increased above I_{BM} ,V_{BE} increases, the collector current increases and V_{CE} falls belowV_{BE} . This continues until the CBJ is forward biased with V_{BC} of about 0.4 to 0.5V, the transistor than goes into saturation. The transistor saturation may be defined as the point above which any increase in the base current does not increase the collector current significantly.

In saturation, the collector current remains almost constant. If the collector emitter voltage is V_{CEsat} the collector current is

$$I_{CS} = \frac{V_{CC} - V_{CESAT}}{R_C}$$

$$I_{BS} = \frac{I_{CS}}{\beta}$$

Normally the circuit is designed so that I_B is higher that I_{BS} . The ratio of I_B to I_{BS} is called to overdrive factor ODF.

$$ODF = \frac{I_B}{I_{BS}}$$

The ratio of I_{CS} to I_B is called as forced β .

$$\beta_{forced} = \frac{I_{CS}}{I_B}$$

2.4 Switching Characteristics

A forward biased p-n junction exhibits two parallel capacitances; a depletion layer capacitance and a diffusion capacitance. On the other hand, a reverse biased p-n junction has only depletion capacitance. Under steady state the capacitances do not play any role. However under transient conditions, they influence turn-on and turn-off behavior of the transistor.

$$I_{BS} = \frac{V_B - V_{BE(sat)}}{\quad} = \frac{5 - 0.7}{\quad} = 4.76mA$$

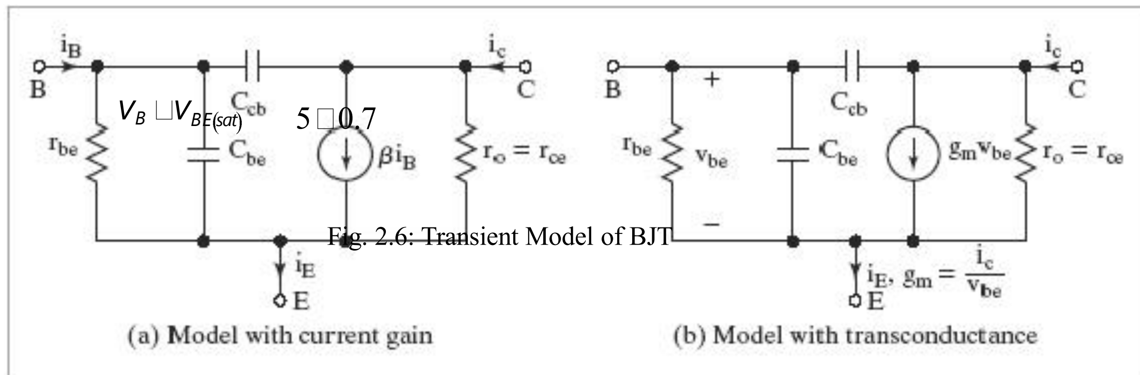


Fig. 2.6: Transient Model of BJT

The drift region in a power transistor is introduced in order to block large forward voltage. However, one effect of introducing the drift region is the appearance of a “quasi saturation region” in the output i-v characteristics of a power transistor. In the quasi saturation state the drift region is not completely shorted out by “conductivity modulation” by excess carriers from the base region. In offers a resistance which is a function of the base current. Although the base current retain some control over collector current in this state the value of dc current gain reduces substantially due to increased effective base width. Another effect of introducing the drift region is to make the VCE saturation voltage depend linearly on the collector current in the hard saturation region due to the ohmic resistance of the “conductivity modulated” drift region.

FBOSOA compactly represents the safe operating limits of a power transistor in terms of maximum forward current, maximum forward voltage, maximum average & instantaneous power dissipation and second break down limits. It is most useful in designing the switching trajectory of a power transistor

For safe switching operation, however it is not sufficient to merely restrict the switching power loss. It will be necessary to restrict the switching trajectory (an instantaneous plot of ic vs VCE during switching with time as a parameter) within the FBSOA /RBSOA region corresponding to a pulse width greater than TSW (ON) or TSW (OFF)

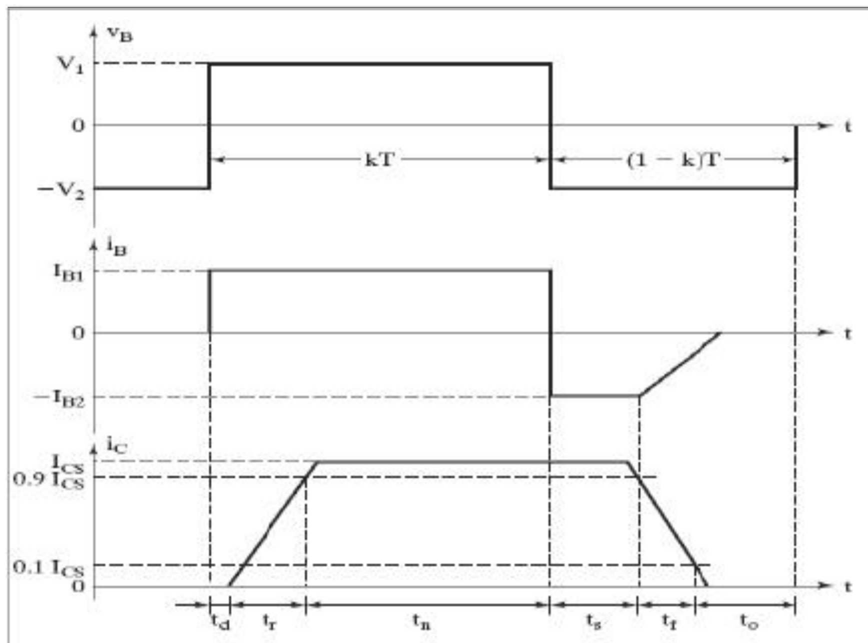


Fig. 2.7: Switching Times of BJT

Due to internal capacitances, the transistor does not turn on instantly. As the voltage V_B rises from zero to V_1 and the base current rises to I_{B1}, the collector current does not respond immediately. There is a delay known as delay time td, before any collector current flows. The delay is due to the time required to charge up the BEJ to the forward bias voltage V_{BE}(0.7V). The collector current rises to the steady value of I_{CS} and this time is called rise time t_r.

The base current is normally more than that required to saturate the transistor. As a result excess minority carrier charge is stored in the base region. The higher the ODF, the greater is the amount of extra charge stored in the base. This extra charge which is called the saturating charge is proportional to the excess base drive.

This extra charge which is called the saturating charge is proportional to the excess base drive and the corresponding current I_e.

$$I_e = I_B - \frac{I_{CS}}{\beta} = ODF.I_{BS} - I_{BS} = I_{BS} \ ODF - 1$$

When the input voltage is reversed from V_1 to $-V_2$, the reverse current $-I_{B2}$ helps to discharge the base. Without $-I_{B2}$ the saturating charge has to be removed entirely due to recombination and the storage time t_s would be longer.

Once the extra charge is removed, BEJ charges to the input voltage $-V_2$ and the base current falls to zero. t_f depends on the time constant which is determined by the reverse biased BEJ capacitance.

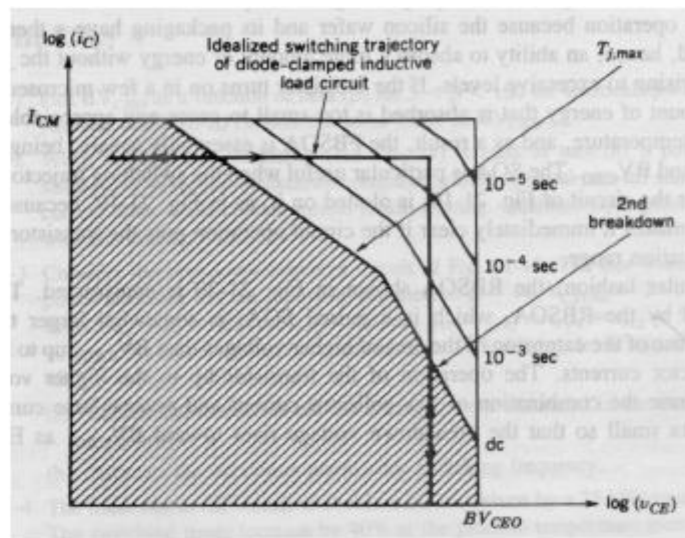
2.5Switching Limits

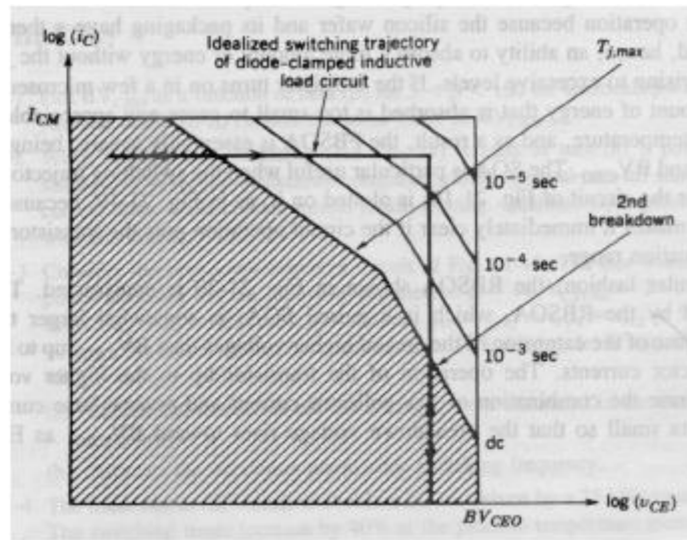
1. Second Breakdown

It is a destructive phenomenon that results from the current flow to a small portion of the base, producing localized hot spots. If the energy in these hot spots is sufficient the excessive localized heating may damage the transistor. Thus secondary breakdown is caused by a localized thermal runaway. The SB occurs at certain combinations of voltage, current and time. Since time is involved, the secondary breakdown is basically an energy dependent phenomenon.

2. Forward Biased Safe Operating Area FBSOA

During turn-on and on-state conditions, the average junction temperature and second breakdown limit the power handling capability of a transistor. The manufacturer usually provides the FBSOA curves under specified test conditions. FBSOA indicates the $I_c - V_{ce}$ limits of the transistor and for reliable operation the transistor must not be subjected to greater power dissipation than that shown by the FBSOA curve.





The dc FBSOA is shown as shaded area and the expansion of the area for pulsed operation of the BJT with shorter switching times which leads to larger FBSOA. The second break down boundary represents the maximum permissible combinations of voltage and current without getting into the region of $i_c - v_{ce}$ plane where second breakdown may occur. The final portion of the boundary of the FBSOA is breakdown voltage limit BV_{CEO}.

3. Reverse Biased Safe Operating Area RBSOA

During turn-off, a high current and high voltage must be sustained by the transistor, in most cases with the base-emitter junction reverse biased. The collector emitter voltage must be held to a safe level at or below a specified value of collector current. The manufacturer provide $I_c - V_{ce}$ limits during reverse-biased turn off as reverse biased safe area (RBSOA).

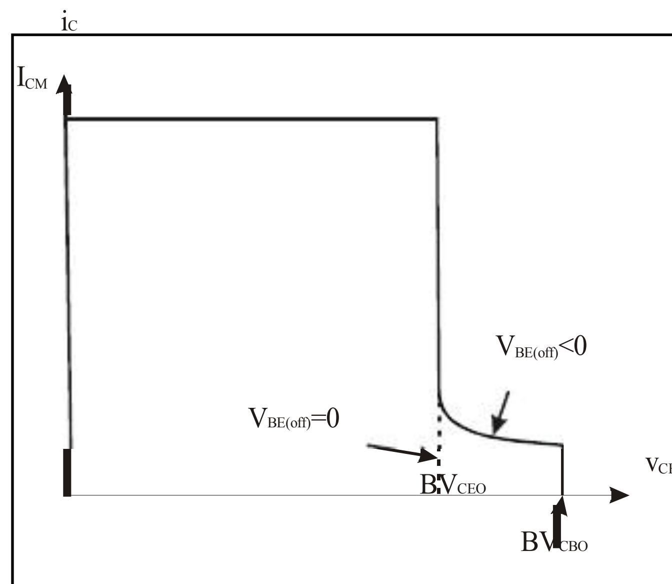


Fig.2.8: RBSOA of a Power BJT

The area encompassed by the RBSOA is somewhat larger than FBSOA because of the extension of the area of higher voltages than BV_{CEO} upto BV_{CBO} at low collector currents.

This operation of the transistor upto higher voltage is possible because the combination of low collector current and reverse base current has made the beta so small that break down voltage rises towards BV_{CBO}.

4. Power Derating

The thermal equivalent is shown. If the total average power loss is P_T,

The case temperature is $T_c = T_j - P T_{jc}$.

The sink temperature is $T_s = T_c - P T_{CS}$

The ambient temperature is $T_A \ T_S - P_T R_{SA}$ and $T_j - T_A$

The maximum power dissipation in P is specified at $T_C = 25^0 C$.

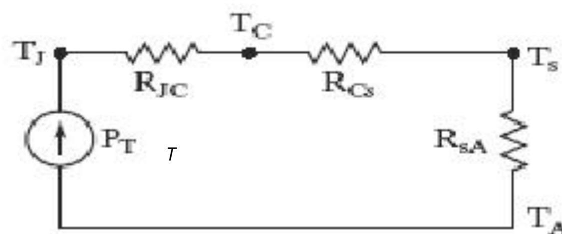


Fig.2.9: Thermal Equivalent Circuit of Transistor

5. Breakdown Voltages

A break down voltage is defined as the absolute maximum voltage between two terminals with the third terminal open, shorted or biased in either forward or reverse direction.

BV_{SUS} : The maximum voltage between the collector and emitter that can be sustained across the transistor when it is carrying substantial collector current.

BV_{CEO} : The maximum voltage between the collector and emitter terminal with base open circuited.

BV_{CBO} : This is the collector to base break down voltage when emitter is open circuited.

6. Base Drive Control

This is required to optimize the base drive of transistor. Optimization is required to increase switching speeds. t_{on} can be reduced by allowing base current peaking during turn-

be increased to a sufficiently high value to maintain the transistor in quasi-saturation region. t_{off} can be reduced by reversing base current and allowing base current peaking during turn off since increasing I_{B2} decreases storage time.

A typical waveform for base current is shown.

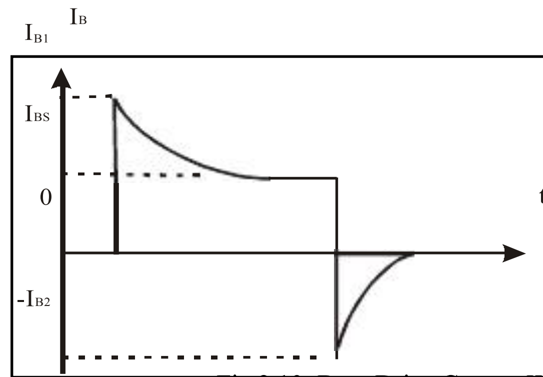


Fig.2.10: Base Drive Current Waveform

Some common types of optimizing base drive of transistor are

- Turn-on Control.
- Turn-off Control.
- Proportional Base Control.
- Antisaturation Control

Turn-On Control

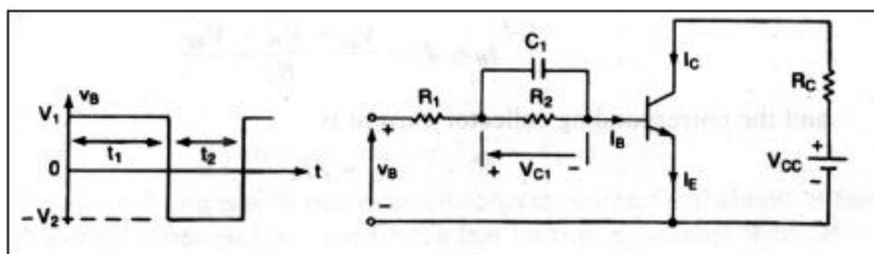


Fig. 2.11: Base current peaking during turn-on

Turn-Off Control

If the input voltage is changed to during turn-off the capacitor voltage V_C is added to V_2 as reverse voltage across the transistor. There will be base current peaking during turn off. As the capacitor C_1 discharges, the reverse voltage will be reduced to a steady state value, V_2. If different turn-on and turn-off characteristics are required, a turn-off circuit using $C_2, R_3 \& R_4$ may be added. The diode D_1 isolates the forward base drive circuit from the reverse base drive circuit during turn off.

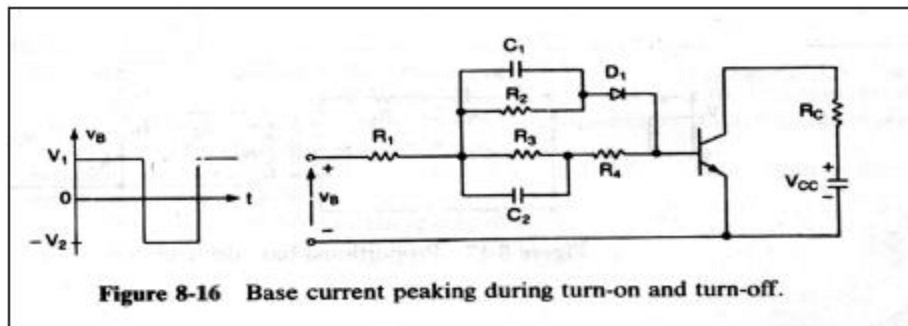


Figure 8-16 Base current peaking during turn-on and turn-off.

Fig: 2.12. Base current peaking during turn-on and turn-off

Proportional Base Control

This type of control has advantages over the constant drive circuit. If the collector current changes due to change in load demand, the base drive current is changed in proportion to collector current.

When switch S_1 is turned on a pulse current of short duration would flow through the base of transistor Q_1 and Q_1 is turned on into saturation. Once the collector current starts to flow, a corresponding base current is induced due to transformer action. The transistor would latch on itself and S_1 can be turned off. The turns ratio is $\frac{N_2}{N_1}$ $\frac{I_C}{I_B}$

of the circuit, the magnetizing current which must be much smaller than the collector current should be as small as possible. The switch S_1 can be implemented by a small signal trans

and additional arrangement is necessary to discharge capacitor C_1 and reset the transformer core during turn-off of the power transistor.

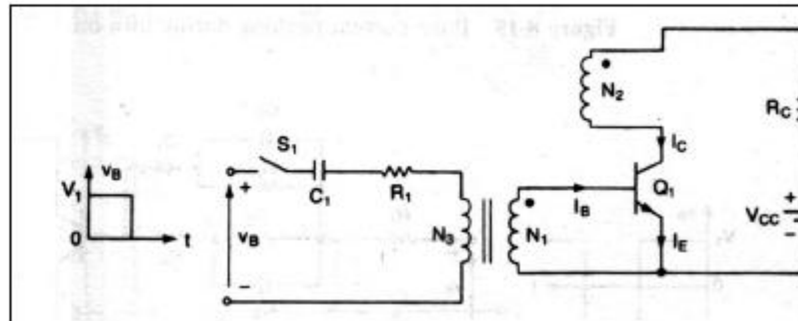


Fig.2.13: Proportional base drive circuit

Antisaturation Control

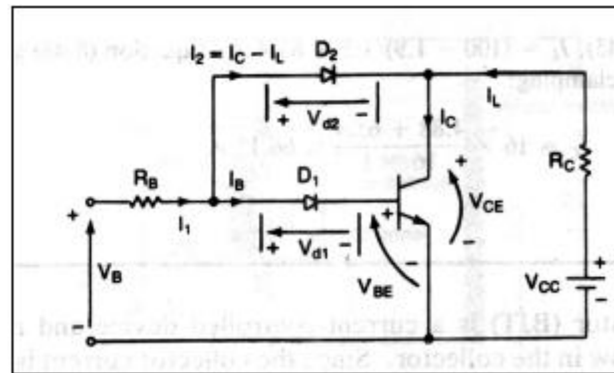


Fig:2.14: Collector Clamping Circuit

If a transistor is driven hard, the storage time which is proportional to the base current increases and the switching speed is reduced. The storage time can be reduced by operating the transistor in soft saturation rather than hard saturation. This can be accomplished by clamping CE voltage to a pre-determined level and the collector current is given by $I_C = \frac{V_{CC} - V_{CM}}{R_C}$.

Where V_{CM} is the clamping voltage and $V_{CM}\ V_{CE}$.

The base current which is adequate to drive the transistor hard, can be found from $I_B = I_1 = \frac{V_B - V_{D1} - V_{BE}}{R_B}$ and the corresponding collector current is $I_C\ I_L\ I_B$.

The clamping action thus results a reduced collector current and almost elimination of the storage time. At the same time, a fast turn-on is accomplished.

However, due to increased V_{CE} , the on-state power dissipation in the transistor is increased, whereas the switching power loss is decreased.

ADVANTAGES OF BJT'S

- BJT's have high switching frequencies since their turn-on and turn-off time is low.
- The turn-on losses of a BJT are small.
- BJT has controlled turn-on and turn-off characteristics since base drive control is possible.
- BJT does not require commutation circuits.

DEMERITS OF BJT

- Drive circuit of BJT is complex.
- It has the problem of charge storage which sets a limit on switching frequencies.

It cannot be used in parallel operation due to problems of negative temperature coefficient.

2.6 POWER MOSFETS

MOSFET stands for metal oxide semiconductor field effect transistor. There are two types of MOSFET

- Depletion type MOSFET
- Enhancement type MOSFET

Depletion Type MOSFET

Construction

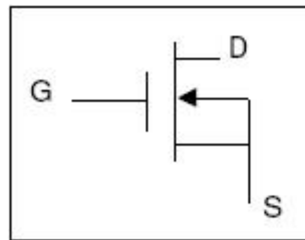


Fig.2.15 Symbol of n-channel depletion type MOSFET

It consists of a highly doped p-type substrate into which two blocks of heavily doped n-type material are diffused to form a source and drain. A n-channel is formed by diffusing between source and drain. A thin layer of SiO_2 is grown over the entire surface and holes are cut in SiO_2 to make contact with n-type blocks. The gate is also connected to a metal contact surface but remains insulated from the n-channel by the SiO_2 layer. SiO_2 layer results in an extremely high input impedance of the order of 10^{10} to $10^{15}\,\Omega$ for this area.

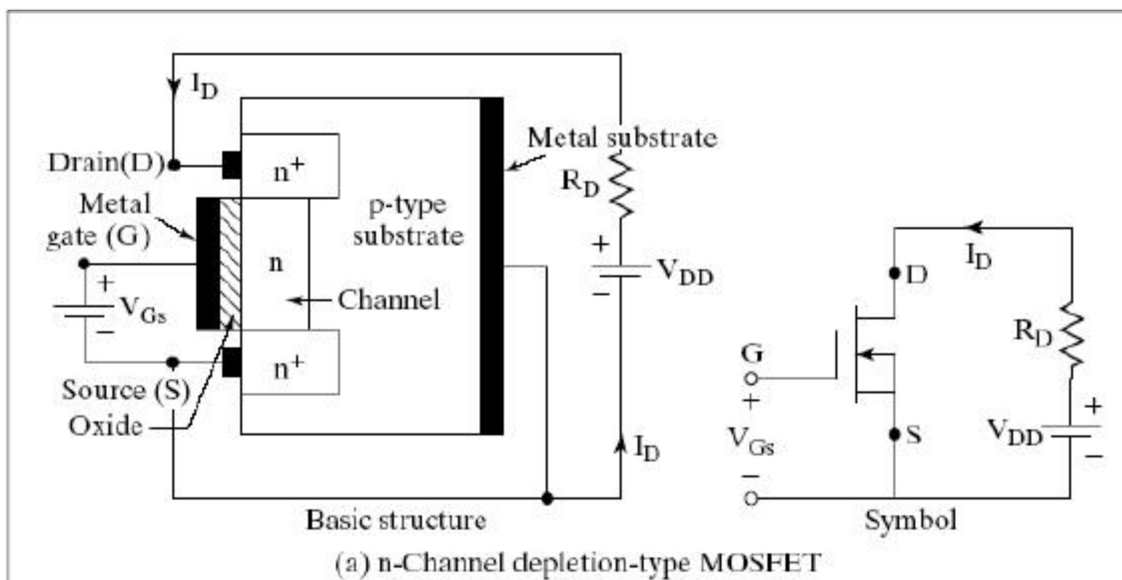


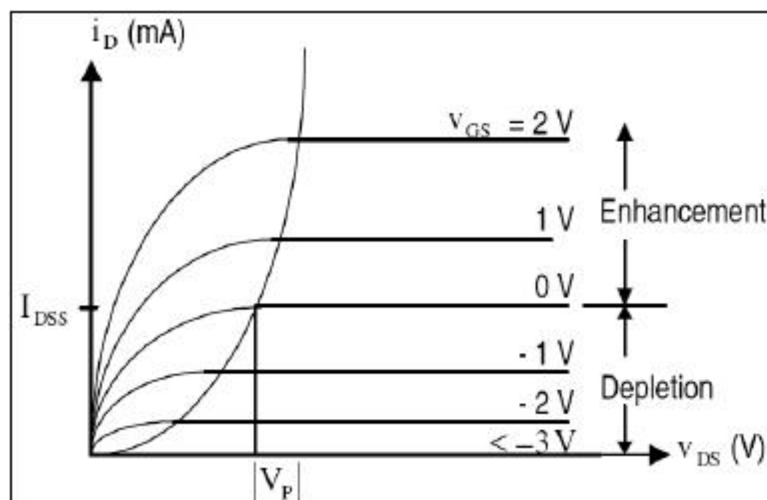
Fig.2.16: Structure of n-channel depletion type MOSFET

Operation

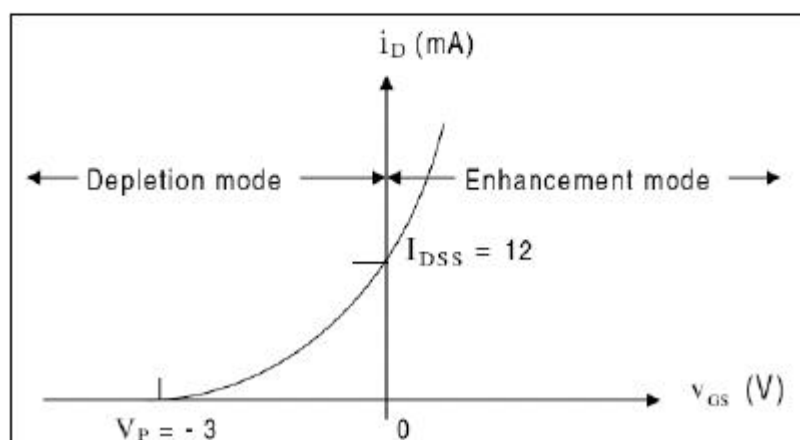
When V_{GS} □ $0V$ and V_{DS} is applied and current flows from drain to source similar to JFET. When V_{GS} □ $-1V$, the negative potential will tend to pressure electrons towards the p-type substrate and attracts hole from p-type substrate. Therefore recombination occurs and will reduce the number of free electrons in the n-channel for conduction. Therefore with increased negative gate voltage I_D reduces.

For positive values, V_{gs}, additional electrons from p-substrate will flow into the channel and establish new carriers which will result in an increase in drain current with positive gate voltage.

Drain Characteristics



Transfer Characteristics

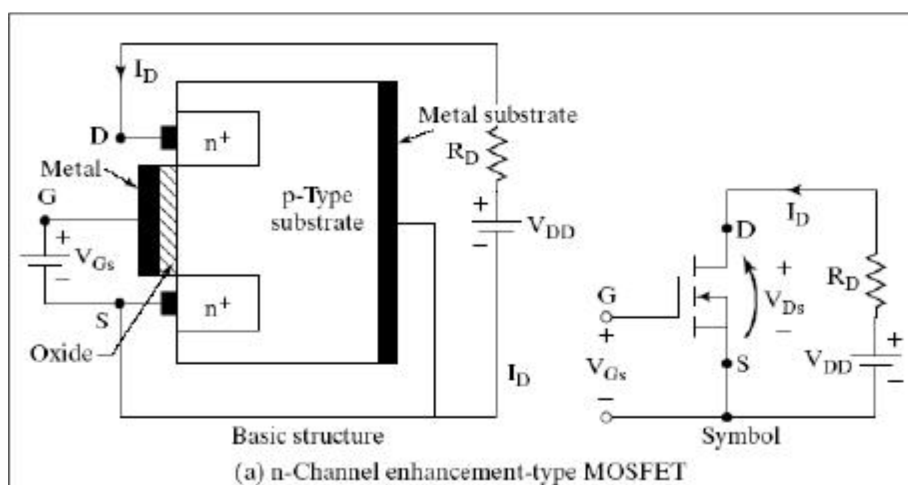


Enhancement Type MOSFET

Here current control in an n-channel device is now affected by positive gate to source voltage rather than the range of negative voltages of JFET's and depletion type MOSFET.

Basic Construction

A slab of p-type material is formed and two n-regions are formed in the substrate. The source and drain terminals are connected through metallic contacts to n-doped regions, but the absence of a channel between the doped n-regions. The SiO_2 layer is still present to isolate the gate metallic platform from the region between drain and source, but now it is separated by a section of p-type material.



(a) n-Channel enhancement-type MOSFET

Fig. 2.17: Structure of n-channel enhancement type MOSFET

Operation

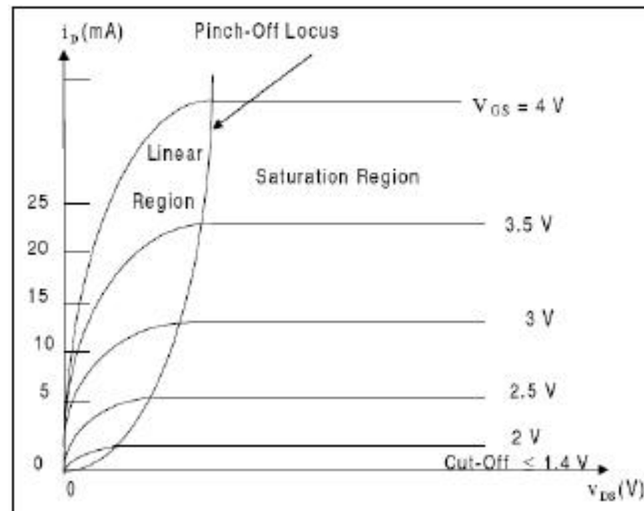
If $V_{GS} = 0V$ and a voltage is applied between the drain and source, the absence of a n-channel will result in a current of effectively zero amperes. With V_{DS} set at some positive voltage and V_{GS} set at 0V, there are two reverse biased p-n junction between the n-doped regions and p substrate to oppose any significant flow between drain and source.

If both V_{DS} and V_{GS} have been set at some positive voltage, then positive potential at the gate will pressure the holes in the p-substrate along the edge of SiO_2 layer to leave the area and enter deeper region of p-substrate. However the electrons in the p-substrate will be attracted to the positive gate and accumulate in the region near the surface of the SiO_2 layer. The negative carriers will not be absorbed due to insulating SiO_2 layer, forming an inversion layer which results in current flow from drain to source.

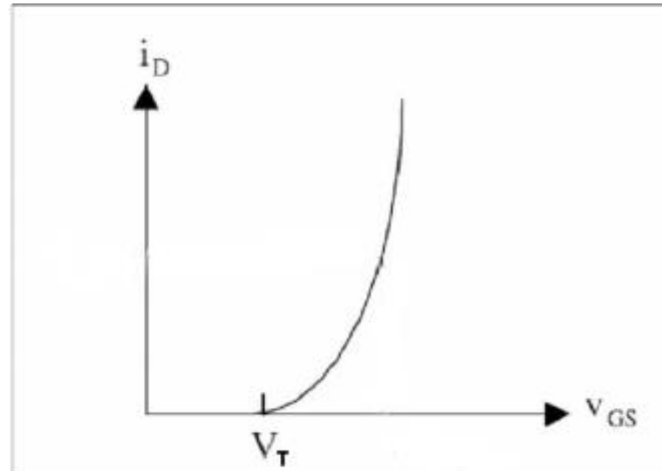
The level of V_{GS} that result in significant increase in drain current is called threshold voltageV_T. As V_{GS} increases the density of free carriers will increase resulting in increased

level of drain current. If V_{GS} is constant V_{DS} is increased; the drain current will eventually reach a saturation level as occurred in JFET.

Drain Characteristics



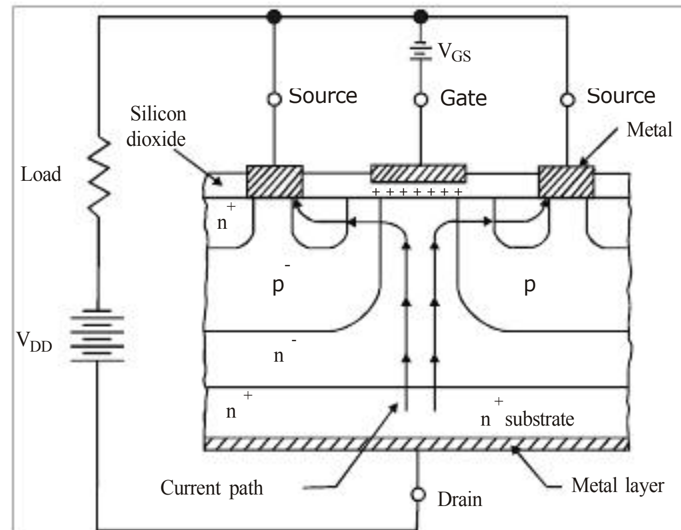
Transfer Characteristics



Power MOSFET'S

Power MOSFET's are generally of enhancement type only. This MOSFET is turned 'ON' when a voltage is applied between gate and source. The MOSFET can be turned 'OFF' by removing the gate to source voltage. Thus gate has control over the conduction of the MOSFET. The turn-on and turn-off times of MOSFET's are very small. Hence they operate at very high frequencies; hence MOSFET's are preferred in applications such as choppers and inverters. Since only voltage drive (gate-source) is required, the drive circuits of MOSFET are very simple. The paralleling of MOSFET's is easier due to their positive

temperature coefficient. But MOSFTS's have high on-state resistance hence for higher currents; losses in the MOSFET's are substantially increased. Hence MOSFET's are used for low power applications.



Construction

Power MOSFET's have additional features to handle larger powers. On the n substrate high resistivity n^- layer is epitaxially grown. The thickness of n^- layer determines the voltage blocking capability of the device. On the other side of n substrate, a metal layer is deposited to form the drain terminal. Now p^- regions are diffused in the epitaxially grown n^- layer. Further n regions are diffused in the p^- regions as shown. SiO_2 layer is added, which is then etched so as to fit metallic source and gate terminals.

A power MOSFET actually consists of a parallel connection of thousands of basic MOSFET cells on the same single chip of silicon.

When gate circuit voltage is zero and V_{DD} is present, $n - p^-$ junctions are reverse biased and no current flows from drain to source. When gate terminal is made positive with respect to source, an electric field is established and electrons from n^- channel in the p^- regions. Therefore a current from drain to source is established.

Power MOSFET conduction is due to majority carriers therefore time delays caused by removal of recombination of minority carriers is removed.

Because of the drift region the ON state drop of MOSFET increases. The thickness of the drift region determines the breakdown voltage of MOSFET. As seen a parasitic BJT is formed, since emitter base is shorted to source it does not conduct.

Switching Characteristics

The switching model of MOSFET's is as shown in the figure 6(a). The various inter electrode capacitance of the MOSFET which cannot be ignored during high frequency

switching are represented by C_{gs}, C_{gd} & C_{ds}. The switching waveforms are as shown in figure 7. The turn on time t_d is the time that is required to charge the input capacitance to the threshold voltage level. The rise time t_r is the gate charging time from this threshold level to the full gate voltage V_{gsp}. The turn off delay time t_{doff} is the time required for the input capacitance to discharge from overdriving the voltage V_1 to the pinch off region. The fall time is the time required for the input capacitance to discharge from pinch off region to the threshold voltage. Thus basically switching ON and OFF depend on the charging time of the input gate capacitance.

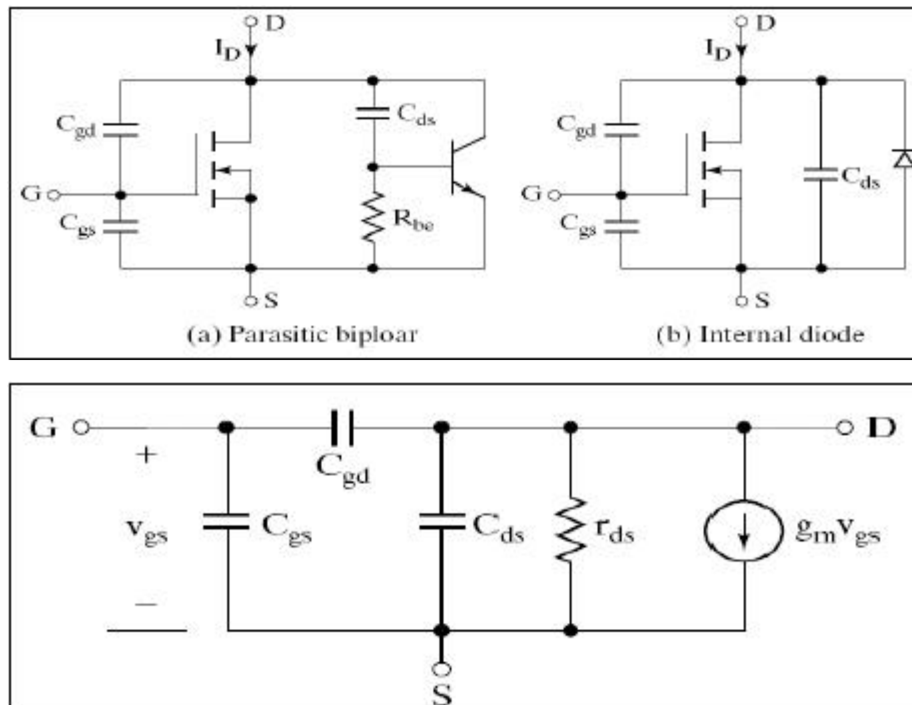


Fig.2.18: Switching model of MOSFET

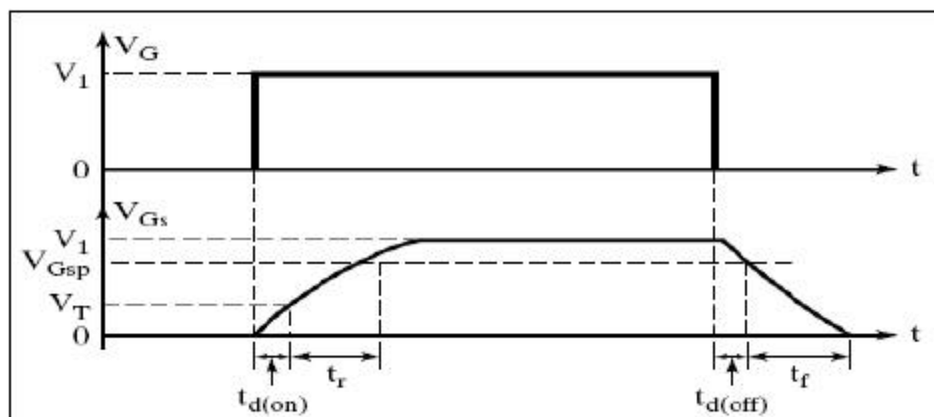


Fig2.19: Switching waveforms and times of Power MOSFET

Gate Drive

The turn-on time can be reduced by connecting a RC circuit as shown to charge the capacitance faster. When the gate voltage is turned on, the initial charging current of the capacitance is

$$I_G = \frac{V_G}{R_S}.$$

The steady state value of gate voltage is

$$V_{GS} = \frac{R_G V_G}{R_S + R_1 / R_G}.$$

Where R_S is the internal resistance of gate drive force.

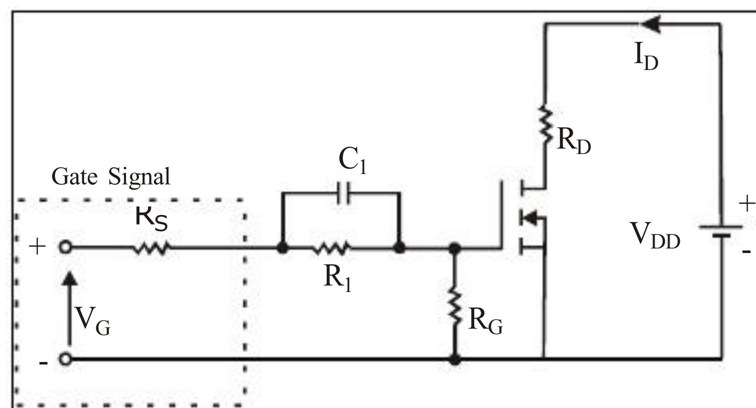


Fig.2.20: Fast turn on gate drive circuit 1

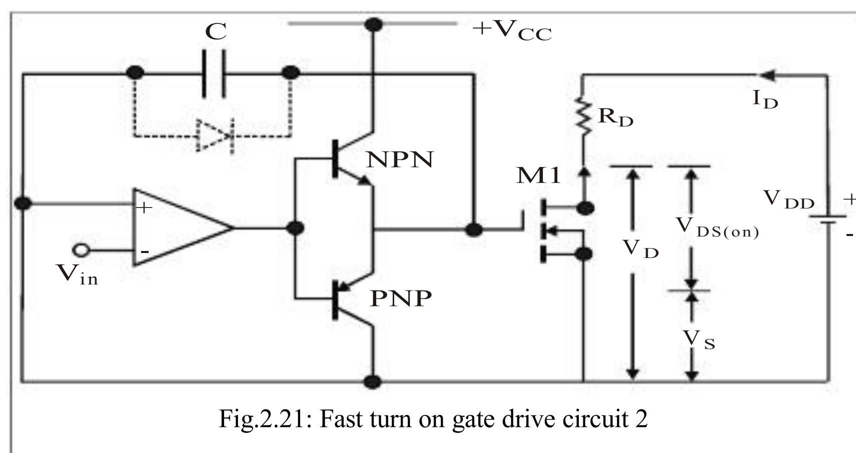


Fig.2.21: Fast turn on gate drive circuit 2

The above circuit is used in order to achieve switching speeds of the order of 100nsec or less. The above circuit as low output impedance and the ability to sink and source large currents. A totem poll arrangement that is capable of sourcing and sinking a large current is achieved by the PNP and NPN transistors. These transistors act as emitter followers and offer a low output impedance. These transistors operate in the linear region therefore minimize the

delay time. The gate signal of the power MOSFET may be generated by an op-amp. Let V_{in} be a negative voltage and initially assume that the MOSFET is off therefore the non-inverting terminal of the op-amp is at zero potential. The op-amp output is high therefore the NPN transistor is on and is a source of a large current since it is an emitter follower. This enables the gate-source capacitance C_{gs} to quickly charge upto the gate voltage required to turn-on the power MOSFET. Thus high speeds are achieved. When V_{in} becomes positive the output of op-amp becomes negative the PNP transistor turns-on and the gate-source capacitor quickly discharges through the PNP transistor. Thus the PNP transistor acts as a current sink and the MOSFET is quickly turned-off. The capacitor C helps in regulating the rate of rise and fall of the gate voltage thereby controlling the rate of rise and fall of MOSFET drain current. This can be explained as follows

- The drain-source voltage $V_{DS} = V_{DD} - I_D R_D$.
- If I_D increases V_{DS} reduces. Therefore the positive terminal of op-amp which is tied to the source terminal of the MOSFET feels this reduction and this reduction is transmitted to gate through the capacitor 'C' and the gate voltage reduces and the drain current is regulated by this reduction.

Comparison of MOSFET with BJT

- Power MOSFETS have lower switching losses but its on-resistance and conduction losses are more. A BJT has higher switching loss bit lower conduction loss. So at high frequency applications power MOSFET is the obvious choice. But at lower operating frequencies BJT is superior.
- MOSFET has positive temperature coefficient for resistance. This makes parallel operation of MOSFET's easy. If a MOSFET shares increased current initially, it heats up faster, its resistance increases and this increased resistance causes this current to shift to other devices in parallel. A BJT is a negative temperature coefficient, so current shaving resistors are necessary during parallel operation of BJT's.
- In MOSFET secondary breakdown does not occur because it have positive temperature coefficient. But BJT exhibits negative temperature coefficient which results in secondary breakdown.
- Power MOSFET's in higher voltage ratings have more conduction losses.
- Power MOSFET's have lower ratings compared to BJT's . Power MOSFET's $\longrightarrow$ 500V to 140A, BJT $\longrightarrow$ 1200V, 800A.

2.7Recommended questions:

1. Explain the control characteristics of the following semiconductor devices
    1) Power BJT 3) MOSFET 4) IGBT
2. Give the comparison between MOSFET and BJT.
3. Draw the circuit symbol of IGBT. Compare its advantages over MOSFET

4. Draw the switching model and switching waveforms of a power MOSFET, define the various switching applications.
5. With a circuit diagram and waveforms of base circuit voltage, base current and collector current under saturation for a power transistor, show the delay that occurs during the turn-ON and turn – OFF.
6. Explain the terms Overdrive factor (ODF) and forced beta for a power transistor for switching applications?
7. Explain the switching characteristics of BJT.
8. Explain the steady and switching characteristics of MOSFET.

2.8 Generic Skills / Outcomes:

- Explain steady state, switching characteristics and gate control requirements of different power transistors and their limitations.

2.9 Further Reading

1. http://books.google.co.in/books/about/Power_Electronics.html?id=-WqvjxMXClAC
2. http://www.flipkart.com/power-electronic-2ed/p/itmczynuyqnbvzzj
3. http://www.scribd.com/doc/36550374/Power-Electronics-Notes
4. http://elearning.vtu.ac.in/EC42.html
5. http://www.onlinevideolecture.com/electrical-engineering/nptel-iit-bombay/power-electronics/?course_id=510