Module-3

General Amplifiers

Darlington Amplifier:

It consists of two emitter followers in cascaded mode as shown in **fig. 1**. The overall gain is close to unity. The main advantage of Darlington amplifier is very large increase in input impedence and an equal decrease in output impedance **.**

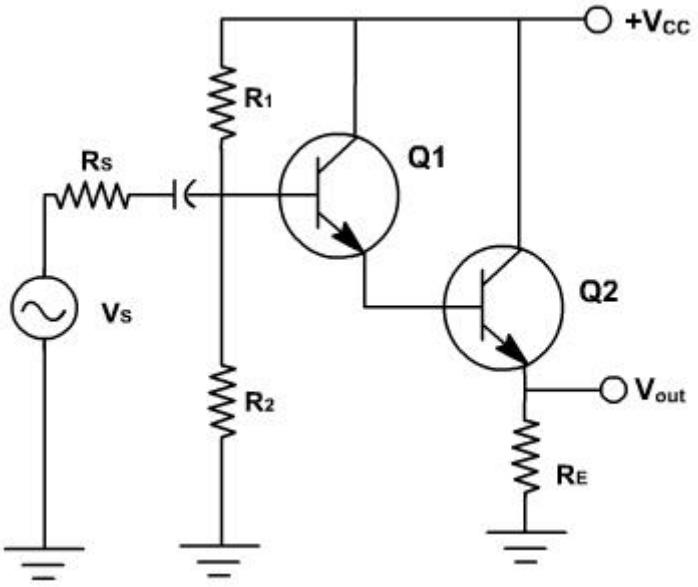

Fig. 1

DC Analysis:

The first transistor has one V_{BE} drop and second transistor has second V_{BE} drop. The voltage divider produces V_{TH} to the input base. The dc emitter current of the second stage is

$I_{E2} = (V_{TH} ? 2\ v_{BE}) / (R_E)$

The dc emitter current of the first stage that is the base current of second stage is given by

$I_{E1} \square I_{E2}./\square_2$

If $r'_{e(2)}$ is neglected then input impedance of second stage is

$Z_{in\,(2)} = \beta_2 R_E$

This is the impedance seen by the first transistor. If $r'_{e(1)}$ is also neglected then the input impedance of 1 becomes.

$Z_{in\,(1)} = \beta_1 \beta_2 R_E$

which is extremely high because of the products of two betas, so the approximate input impedance of Darlington amplifier is

$Z_{in} = R_1 \parallel R_2$

Output impedance:

The Thevenin impedance at the input is given by

$R_{TH} = R_S \parallel R_1 \parallel R_2$

Similar to single stage common collector amplifier, the output impedance of the two stages $z_{out(1)}$ and $z_{out(2)}$ are given by.

$$z_{out1} = r'_{e1} + \frac{R_{TH}}{\beta_1}$$

$$z_{out2} = r'_{e2} + \frac{z_{out1}}{\beta_2}$$

$$= r'_{e2} + \frac{r'_{e1} + \frac{R_{TH}}{\beta_1}}{\beta_2}$$

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Therefore, t he output impedance of the amplifier is very small.

Efficiency is given by

$$\eta\% = \frac{P_{OUT}}{P_{DC}} \times 100$$

Value is around 40%

Example-1

Design a single stage npn emitter follower amplifier as shown in **fig. 2** with $\beta = 60$, $V_{BE} = 0.7V$, $R_{source} = 1\ K\Omega$, and $V_{CC} = 12V$. Determine the circuit element values for the stage to achieve $A_i = 10$ with a $100\ \Omega$ load.

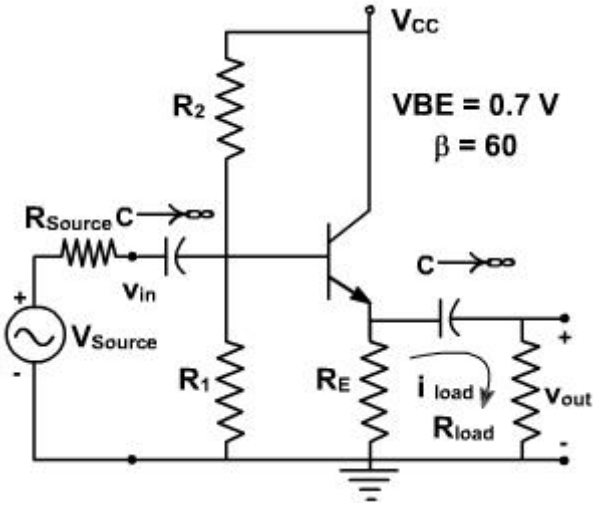


Fig. 2

Solution:

We must select R_1, R_2 and R_E, but we only have two equations. These two equations are specified by the current gain and the placement of the Q-point.

As discussed earlier, the best choice for a CE amplifier is to make $R_C = R_{load}$. We could derive a similar result for R_E and R_{load} in the CC amplifier. We shall therefore begin by constraining $R_E$to be equal to R_{load}. This yields a third equation,

$R_E = R_{load} = 100\ W$

Now finding the load line slopes,

$R_{ac} = R_E \parallel R_{load} = 50\ W$

$R_{dc} = R_E = 100\ V$

Since the amplitude of the input is not specified, we choose the quiescent current to place the Q-point in the center of the ac load line for maximum swing.

$$I_{CQ} = \frac{V_{CC}}{R_{ac} + R_{dc}} = 80\ mA$$

$$V_{CEQ} = I_{CQ} R_{ac} = 4\ V$$

We now find the value of r'_e

$$r_e' = \frac{25\ (mV)}{|I_{CQ}|} = \frac{25\ (mV)}{80\ (mA)} = 0.313\Omega$$

Since r_e is insignificant compared to $R_E \parallel R_{load}$, it can be ignored. This is usually the case for emitter follower circuits.

Using the equation for current gain we find

$$A_i = \frac{\beta R_E R_B}{(R_E + R_{load})[R_B + (R_E \parallel R_{load})\beta]}$$

Everything in this equation is known except R_B. We solve for R_B with the result

$R_B = 1500$ W

V_{BB} is found from the base loop.

$$V_{BB} = V_{BE} + I_{CQ}\left(\frac{R_B}{\beta} + R_E\right) = 10.7\ V$$

Continuing with the design as discussed earlier, we find

$R_1 = 13.8$ K Ω

$R_2 = 1.68$ K Ω

The voltage gain of the CC amplifier is approximately unity.

The input resistance is given by

$R_{in} = R_B \parallel [\ \beta\ (\ R_E \parallel R_{load}\ )\ ] = 1$ kΩ

The output resistance is given by

$$R_O = \left(\frac{R_s + R_{source} \parallel R_B}{\beta}\right) \parallel R_E = 9.36\Omega$$

The maximum peak to peak symmetrical output swing is given by

$V_{out}(p\text{-}p) \approx 1.8 \, |I_{CQ}| \, (R_E \parallel R_{load}) = 7.2$ V

The power dissipated in the load, P_{load}, and the maximum power required of the transistor, $P_{transistor}$, are

$$P_{load} = \frac{(0.9 I_{CQ}/2)^2 R_{load}}{2} = 64.8 \text{ mW}$$

$$P_{transistor} = I_{CQ} V_{CEQ} = 320 \text{ mW}$$

Example-2 (Capacitor-Coupled CB Design)

Design a CB amplifier using an npn transistor as shown in **fig. 3** with $\beta = 100$, $V_{CC} = 24$ V, $R_{load} = 2K\Omega$, $R_E = 400\Omega$ $V_{BE} = 0.7$V. Design this amplifier for a voltage gain of 20.

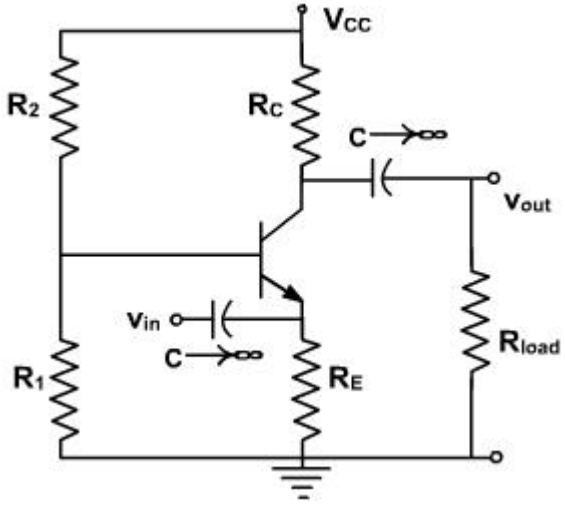


Fig. 3

Solution:

Since there are fewer equations than there are unknowns, we need an additional constraint, so we set

$R_C = R_{load} = 2$ K Ω

Then we have,

$$R_B + r'_E = \frac{R_{load} \,||\, R_C}{A_v} = 50 \ \Omega$$

R_{ac} = 1.40 K Ω and R_{dc} =2.40 KΩ

For maximum swing, we set I_{CQ} to

$$I_{CQ} = \frac{V_{CC}}{R_{ac} + R_{dc}} = 6.30 \ \text{mA}$$

We now find that

$$r_E' = \frac{0.025}{I_C} = 3.97 \ \Omega$$

$$R_B = \beta\,(50 - 3.97) = 4.60 \ \text{K}\Omega$$

The current gain is given by

$$A_i = \frac{400}{400 + 50} \ \frac{2000}{2000 + 2000} = 0.44$$

and input impedance is given by

$$R_{in} = R_E \left\| \left(r_e + \frac{R_B}{\beta} \right) \right. = 44 \ \Omega$$

We use the bias equation to find the parameters of the input bias circuitry.

$$V_{BB} = V_{BE} + I_{CQ}\left(\frac{R_B}{\beta} + R_E \right) = 3.51 \ \text{V}$$

The bias resistors are then given by

$$R_1 = \frac{R_B}{1 - V_{BB}/V_{CC}} = 5.38 \ \text{K}\Omega$$

$$R_2 = \frac{R_B V_{CC}}{V_{BB}} = 31.4 \ \text{K}\Omega$$

The maximum peak-to-peak undistorted output voltage is

V_{out}(peak-peak) = 1.8 | I_{CQ} | (R_{load} || R_C) = 11.3 V

Power rating is an important consideration in selecting bias resistors since they must be capable of withstanding the maximum anticipated (worst case) power without overheating. Power considerations also affect transistor selection. Designers normally select components having the lowest power handling capability suitable for the design. Frequently, de-rating (i.e., providing a "safety margin" from derived values) is used to improve the reliability of a device. This is similar to using safety factors in the design of mechanical systems where the system is designed to withstand values that exceed the maximum.

Consider a common emitter amplifier circuit shown in **fig. 1**.

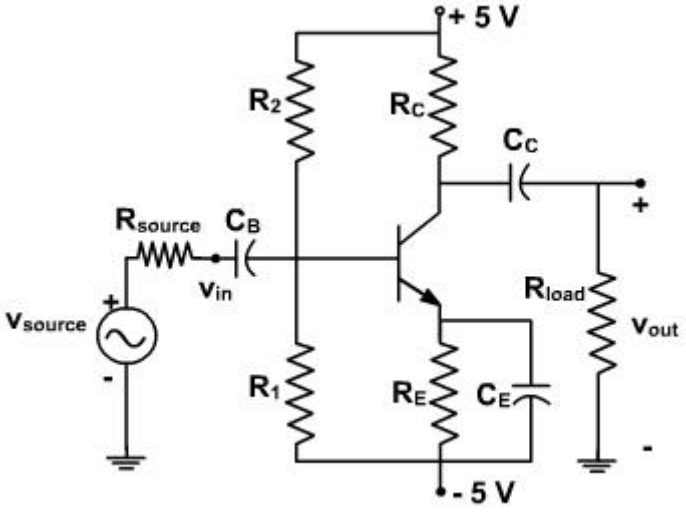


Fig. 1

Derivation of Power Equations

Average power is calculated as follows:

For dc: $$P = VI = I^2R = \frac{V^2}{R} \quad W \qquad \text{(E-1)}$$

For ac: $$P = \frac{1}{T}\int_0^T v(t).\, i(t)\, dt \quad W \qquad \text{(E-2)}$$

In the ac equation, we assume periodic waveforms where T is the period. If the signal is not periodic, we must let T approach infinity in equation E-1. Looking at the CE amplifier of **fig. 1**, the power supplied by the power source is dissipated either in R_1 and R_2 or in the transistor (and its associated collector and emitter circuitry). The power in R_1 and R_2 (the bias circuitry) is given by

$$R_{(bias)} = I^2_{R2} R_2 + I^2_{R1} R_1 \quad \text{(E-3)}$$

where I_{R1} and I_{R2} are the (downward) currents in the two resistors. Kirchhoff's current law (KCL) yields a relationship between these two currents and the base quiescent current.

$I_{R1} = I_{R2} ? I_B$ (E-4)

KVL yields the base loop equation (assuming $V_{EE} = 0$),

$I_{R2} R_2 + I_{R1} R_1 = V_{CC}$ (E-5)

These two equations can be solved for the currents to yield,

$$I_{R1} = \frac{V_{CC} - R_2 I_B}{R_2 + R_1}$$
$$I_{R2} = \frac{V_{CC} - R_1 I_B}{R_2 + R_1} \quad \text{(E-6)}$$

In most practical circuits, the power due to I_B is negligible relative to the power dissipated in the transistor and in R_1 and R_2. We will therefore assume that the power supplied by the source is approximately equal to the power dissipated in the transistor and in R_1 and R_2. This quantity is given by

$$P_{VCC} = \frac{1}{T}\int_0^T V_{CC}\left[I_{CQ} + i_c(t)\right] dt + P_{(bias\,circuit)} = V_{CC} I_{CQ} + \frac{V_{CC}^2}{R_1 + R_2} \quad \text{(E-7)}$$

Where the source voltage V_{CC} is a constant value. The source current has a dc quiescent component designated by i_{CEQ} and the ac component is designated by $i_c(t)$. The last equality of Equation (E-7) assumes that the average value of $i_c(t)$ is zero. This is a reasonable assumption. For example, it applies if the input ac signal is a sinusoidal waveform.

The average power dissipated by the transistor itself (not including any external circuitry) is

$$P(\text{transistor}) = \frac{1}{T}\int_0^T v_{CE}(t)\, i_C(t)\, dt \qquad \text{(E-8)}$$

For zero signal input, this becomes

$P(\text{transitor}) = V_{CEQ}\, I_{CQ}$

Where V_{CEQ} and I_{CQ} are the quiescent (dc) values of the voltage and current, respectively.

For an input signal with maximum possible swing (i.e., Q-point in middle and operating to cutoff and saturation),

$$v_{CE}(t) = V_{CEQ} - V_{CEQ} \sin \omega t = V_{CEQ}\,(1-\sin \omega t) \qquad \text{(E-9)}$$
$$i_c(t) = I_{CQ} + I_{CQ} \sin \omega t = I_{CQ}\,(1+\sin \omega t)$$
$$p(t) = v_{CE}(t)\,.\, i_C(t) = \frac{V_{CEQ}\, I_{CQ}}{2}\,(1+\cos(2\omega t))$$

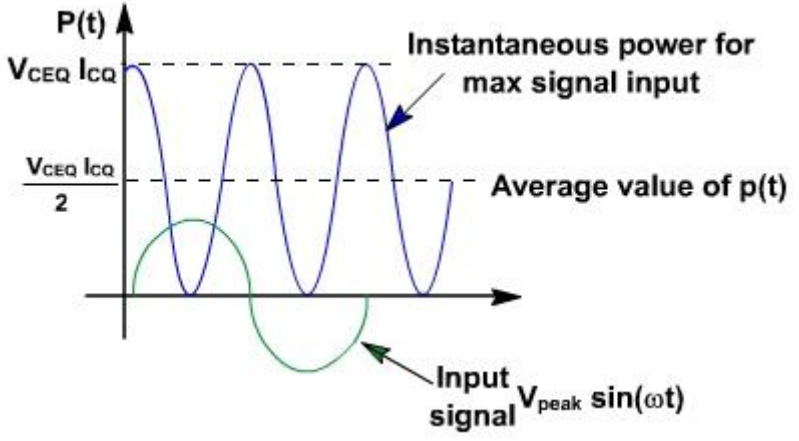


Fig. 2

Putting these time functions in Equation (E-7) yields the power equation,

$$P(\text{transistor}) = \frac{1}{T}\int_0^T V_{CEQ}\, I_{CQ}\left(1-\sin^2\omega t\right)$$
$$= \frac{1}{T}\int_0^T V_{CEQ}\, I_{CQ}\left(\frac{1}{2}+\frac{1}{2}\cos 2\omega t\right)dt = \frac{V_{CEQ}\, I_{CQ}}{2} \qquad \text{(E-10)}$$

From the above derivation, we see that the transistor dissipates its maximum power (worst case) when no ac signal input is applied. This is shown in **fig. 2**, where we note that the frequency of the instantaneous power sinusoid is 2ω.

Depending on the amplitude of the input signal, the transistor will dissipate an average power between V_{CEQ} I_{CQ} and one half of this value. Therefore, the transistor is selected for zero input signal so it will handle the maximum (worst case) power dissipation of V_{CEQ} I_{CQ}.

We will need a measure of efficiency to determine how much of the power delivered by the source appears as signal power at the output. We define conversion efficiency as

$$\eta_{conversion} = \frac{P_{out(ac)}}{P_{in(dc)}} \times 100.$$

Cascade Amplifier:

To increases the voltage gain of the amplifier, multiple amplifier are connects in cascade. The output of one amplifier is the input to another stage. In this way the overall voltage gain can be increased, when number of amplifier stages are used in succession it is called a multistage amplifier or cascade amplifier. The load on the first amplifier is the input resistance of the second amplifier. The various stages need not have the same voltage and current gain. In practice, the earlier stages are often voltage amplifiers and the last one or two stages are current amplifiers. The voltage amplifier stages assure that the current stages have the proper input swing. The amount of gain in a stage is determined by the load on the amplifier stage, which is governed by the input resistance to the next stage. Therefore, in designing or analyzing multistage amplifier, we start at the output and proceed toward the input.

A n-stage amplifier can be represented by the block diagram as shown in **fig. 3**.

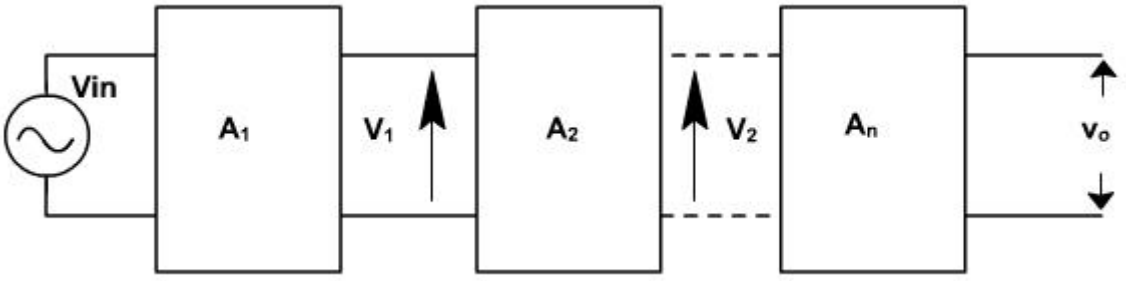


Fig. 3

In **fig. 3**, the overall voltage gain is the product of the voltage gain of each stage. That is, the overall voltage gain is ABC.

To represent the gain of the cascade amplifier, the voltage gains are represents in dB. The two power levels of input and output of an amplifier are compared on a logarithmic scale rather than linear scale. The number of bels by which the output power P_2 exceeds the input power P_1 is defined as

$$\text{No of bels} = \log_{10}\left(\frac{P_2}{P_1}\right)$$

$$\text{or No of dB} = 10 * \text{No. of bels}$$

$$= 10 \log_{10}\left(\frac{P_2}{P_1}\right)$$

Since,

$$P_1 = \frac{v_1^2}{R_{in}} \;\&\; P_2 = \frac{v_2^2}{R_0}$$

where R_{in} is the input resistance of the amplifier and R_0 is the load resistance

$$dB = 10 \log_{10}\left(\frac{v_2^2 / R_0}{v_1^2 / R_{in}}\right)$$

In case R_{in} and R_0 are equal, then power gain is given by

$$dB = 10 \log_{10}\left(\frac{v_2}{v_1}\right)^2 = 20 \log_{10}\left(\frac{v_2}{v_1}\right)$$

$$\therefore A_{dB} = A_{dB1} + A_{dB2} + \ldots\ldots$$

Because of dB scale the gain can be directly added when a number of stages are cascaded.

Types of Coupling:

In a multistage amplifier the output of one stage makes the input of the next stage. Normally a network is used between two stages so that a minimum loss of voltage occurs when the signal passes through this network to the next stage. Also the dc voltage at the output of one stage should not be permitted to go to the input of the next. Otherwise, the biasing of the next stage are disturbed.

The three couplings generally used are.

1. RC coupling
2. Impedance coupling
3. Transformer coupling.

1.RC coupling:

Fig. 4 shows RC coupling the most commonly used method of coupling from one stage to the next. An ac source with a source resistance R S drives the input of an amplifier. The grounded emitter stage amplifies the signal, which is then coupled to next CE stage the signal is further amplified to get larger output.

In this case the signal developed across the collector resistor of each stage is coupled into the base of the next stage. The cascaded stages amplify the signal and the overall gain equals the product of the individual gains.

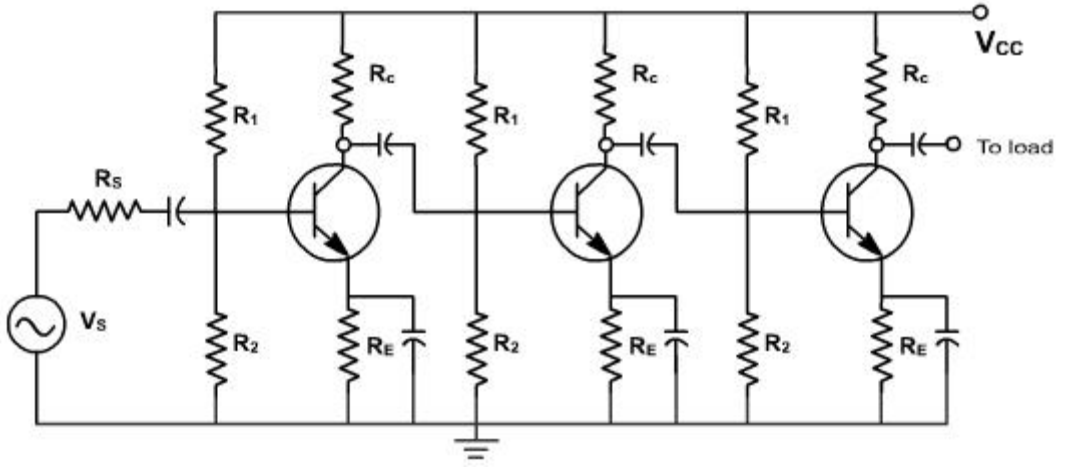


Fig. 4

The coupling capacitors pass ac but block dc Because of this the stages are isolated as for as dc is concerned. This is necessary to avoid shifting of Q-points. The drawback of this approach is the lower frequency limit imposed by the coupling capacitor.

The bypass capacitors are needed because they bypass the emitters to ground. Without them, the voltage gain of each stage would be lost. These bypass capacitors also place a lower limit on the frequency response. As the frequency keeps decreasing, a point is reached at which capacitors no longer look like a.c. shorts. At this frequency the voltage gain starts to decrease because of the local feedback and the overall gain of the amplifier drops significantly. These amplifiers are suitable for frequencies above 10 Hz.

Example - 1

Determine the current and voltage gains for the two-stage capacitor-coupled amplifier shown in **fig. 1**.

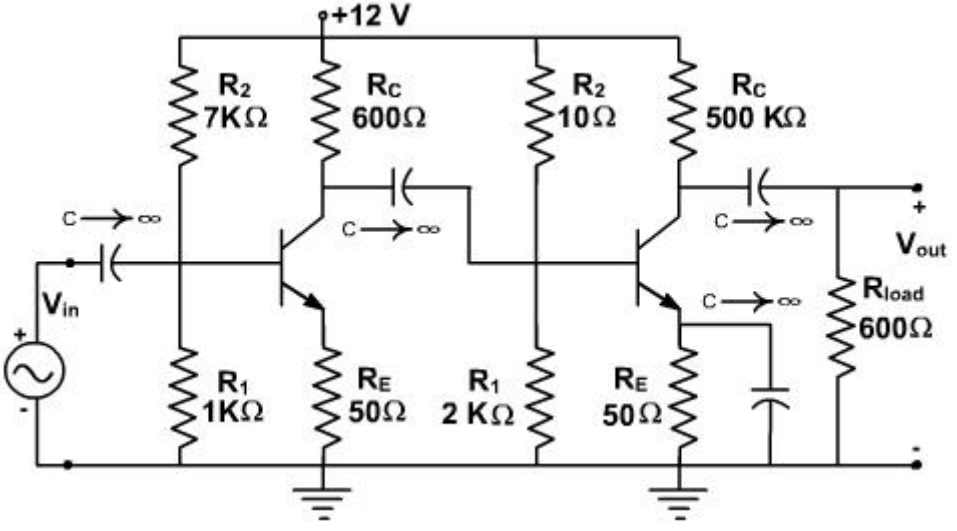


Fig. 1

Solution:

We develop the hybrid equivalent circuit for the multistage amplifier. This equivalent is shown in **fig. 2**. Primed variables denote output stage quantities and unprimed variables denote input stage quantities.

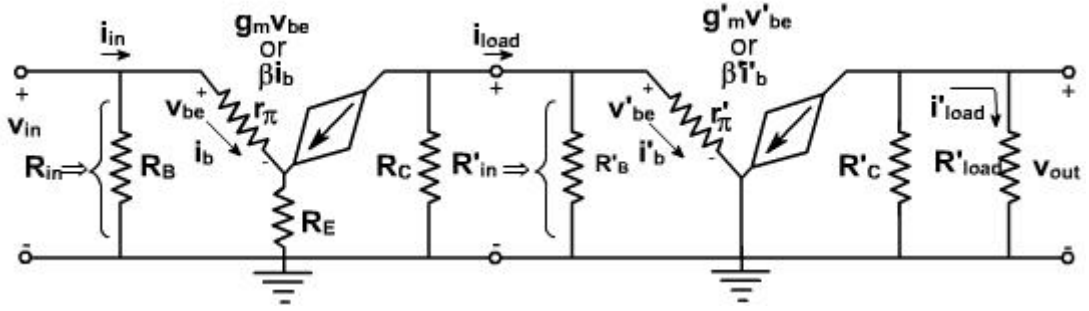


Fig. 2

Calculations for the output stages are as follows

$$R'_B = 10\,K\Omega \parallel 2\,K\Omega = \frac{10^4 \times 2 \times 10^3}{10^4 + 2 \times 10^3} = 1.67\,K\Omega$$

$$V'_{BB} = 12V \times \frac{2\,K\Omega}{10\,K\Omega + 2\,K\Omega} = \frac{12 \times 2 \times 10^3}{10^4 + 2 \times 10^3} = 2\,V$$

$$I'_{CQ} = \frac{V'_{BB} - V_{BE}}{R'_B/\beta + R'_B} = 22\,mA$$

$$r'_e = \frac{26(mV)}{I_{CQ}} = 1.77\ \ \Omega$$

For the input stage,

$$R_B = 7\,K\Omega \parallel 1K\Omega = \frac{7000 \times 1000}{7000 + 1000} = 875\,\Omega$$

$$V_{BB} = 12\,\frac{1K\Omega}{1\,K\Omega + 7\,K\Omega} = \frac{12 \times 1000}{700 + 1000} = 1.5\,V$$

$$I_{CQ} = \frac{1.5 - 0.7}{875/200 + 50} = 14.7\ \ mA$$

$$r_e' = \frac{26\ (mV)}{14.7\ (mA)} = 1.77\,\Omega$$

The input resistance is determined as:

$$R_{in} = R_B \| (r_\pi + \beta R_E) = \frac{875 \times 200 \times (1.77 + 50)}{875 + 10{,}354} = 807\ \Omega$$

The current gain, A_i, can be found by applying the equations derived earlier, where the first stage requires using the correct value for R_{load} derived form the value of R_{in} to the next stage.

Alternatively, we analyze **fig. 2** by extracting four current dividers as shown in **fig. 3**.

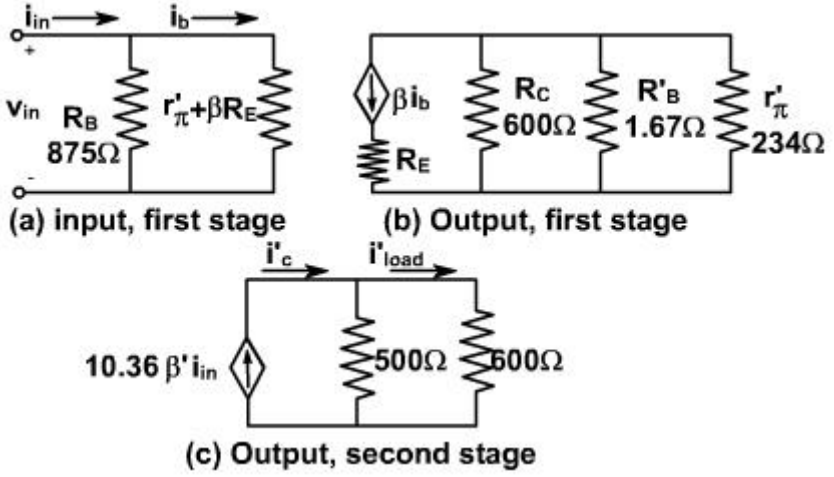


Fig. 3

The current division of the input stage is

$$i_b = \frac{R_B\, i_{in}}{R_B + r_\pi + \beta R_E} = 0.078\ i_{in}$$

The output of the first stage is coupled to the input of he second stage in **fig. 3(b)**. The input resistance of the second stage is

$$R'_{in} = R'_B \| r'_\pi = 205\ \Omega$$

The current in R'_{in} is i_{load} and is given by

$$i_{load} = \frac{15.6\, i_{in} \times 600}{805} = 11.6\, i_{in}$$

Again, i_{load} is current-divided at the input to the second stage. Thus,

$$i'_b = \frac{-R'_B\, i_{load}}{R'_B + r'_\pi} = -10.2\, i_{in}$$

The output current is found from **fig. 3(c)**:

$$i'_{load} = \frac{10.2\, i_{in} \times 200 \times 500}{500 + 600} = 927 \cdot i_{in}$$

The current gain is then

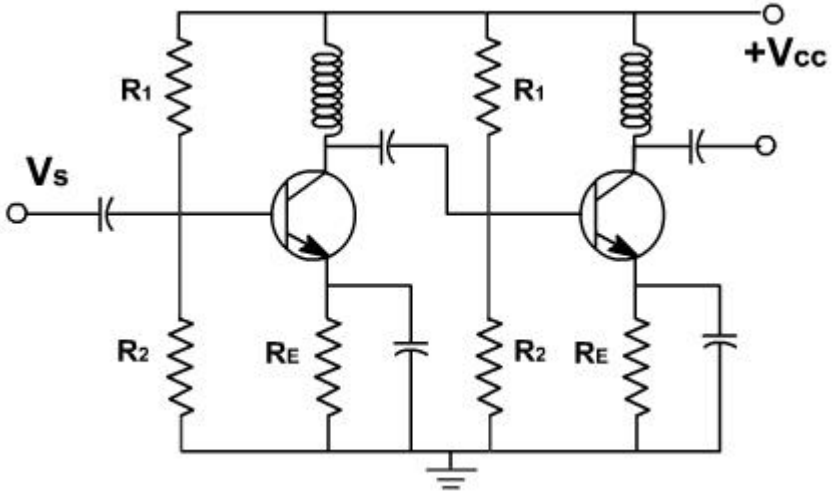
$A_i = 927$

Now using the gain impedance formula, we find the voltage gain:

$$A_v = \frac{927 \times 600}{807} = 689$$

Impedance Coupling:

At higher frequency impedance coupling is used. The collector resistance is replaced by an inductor as shown in **fig. 4**. As the frequency increases, X_L approaches infinity and each inductor appears open. In other words, inductors pass dc but block ac. When used in this way, the inductors are called RFchokes.



The advantage is that no signal power is wasted in collector resistors. These RF chokes are relatively expensive and their impedance drops off at lower frequencies. It is suitable at radio frequency above 20 KHz.

Transformer Coupling:

In this case a transformer is used to transfer the ac output voltage of the first stage to the input of the second stage. **Fig. 5**, the resistors R_C is replaced by the primary winding of the transformer. The secondary winding is used to give input to next stage. There is no coupling capacitor. The dc isolation between the two stages provided by the transformer itself. There is no power loss in primary winding because of low resistance.

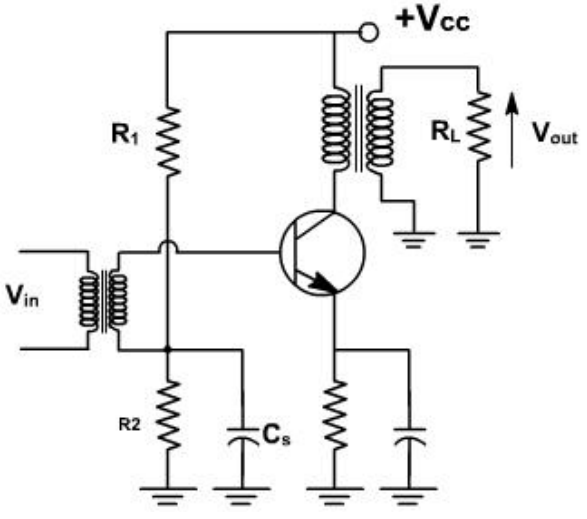


Fig. 5

At low frequency the size and cost of the transformer increases. Transformer coupling is still used in RF amplifiers. In AM radio receivers, RF signal have frequencies 550 to 1600 KHz. In TV receivers, the frequencies are 54 to 216 MHz. At these frequency the size and cost of the transformer reduces. C_S capacitor is used to make other point of transformer grounded, so that ac signal is applied between base and ground.

Tuned Transformer Coupling:

In this case a capacitor is shunted across primary winding to get resonance as shown in **fig. 6**. At this frequency the gain is maximum and at other frequencies the gain reduces very much.

This allows us to filter out all frequencies except the resonant frequency and those near it. This is the principle behind tuning in a radio station or TV channel.

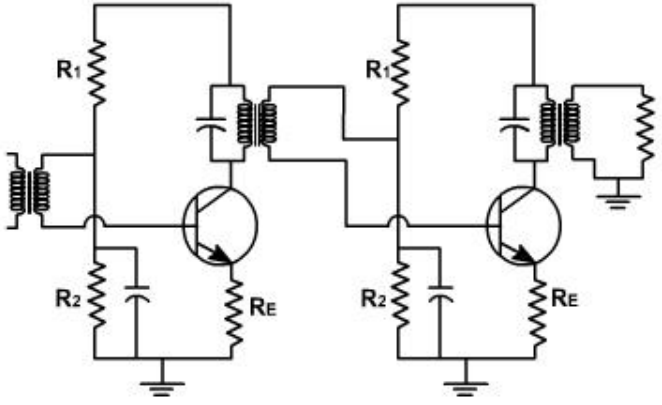


Fig. 6

Example - 2

Design a transformer-coupled amplifier as shown in **fig. 7** for a current gain of $A_i = 80$. Find the power supplied to the load and the power required from the supply.

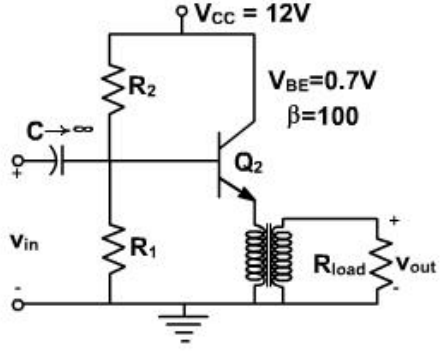


Fig. 7

Solution:

We first use the design equation to find the location of the Q-point for maximum output swing.

$$I_{CQ} = \frac{V_{CC}}{R_{ac} + R_{dc}} = \frac{12}{a^2 R_{load}} = 23.4\text{mA}$$

Since the problem statement requires a current gain of 80, the amplifier must have a current gain of 10 because the transformer provides an additional gain of 8. We use the equations from Chapter 5 to find the base resistance R_B,

$$A_i = \frac{R_B}{R_B/\beta + r_e + R_E} = 10$$

where

$$R_E = a^2 R_{load} = 512\ \Omega$$

We note that r_e is sufficiently small to be neglected. Then, solving for R_B yields

$$R_B = 54.69\ K\Omega$$

$$V_{BB} = \frac{I_{CQ}R_B}{\beta} + V_{BE} = 2.03\ V$$

Now solving for the bias resistors,

$$R_1 = \frac{R_B}{1 + V_{BB}/V_{CC}} = 6.85\ K\Omega$$

$$R_2 = \frac{V_{CC}R_B}{V_{BB}} = 33.6\ K\Omega$$

The design is now complete. The power delivered by the source is given by

$$P_{V_{cc}} = V_{CC}I_{CQ} + \frac{V_{CC}^2}{R_1 + R_2} = 284\ mW$$

The power dissipated in the load is

$$P_{load} = \frac{(0.9a\, I_{CQ})^2\, R_{load}}{2} = 114\ \ mW$$

We have restricted operation to the linear region by eliminating 5% of the maximum swing near cutoff and saturation. The efficiency is the ratio of the load to source power.

$$\eta = \frac{114}{284} = 0.4 \text{ or } 40\ \%$$