University syllabus

Module-1

Diode Circuits: Review of diodes as rectifiers (No question shall be set from review portion). Diode clipping and clamping circuits.

Transistor biasing and stabilization: Operating point, analysis and design of fixed bias circuit, self-bias circuit, Emitter stabilized bias circuit, voltage divider bias circuit, stability factor of different biasing circuits. Problems.

Transistor switching circuits: Transistor switching circuits, PNP transistors, thermal compensation techniques.

Module-2

Transistor at low frequencies: BJT transistor modelling, CE fixed bias configuration, voltage divider bias, emitter follower, CB configuration, collector feedback configuration, analysis using h – parameter model, relation between h – parameters model of CE, CC and CB modes, Millers theorem and its dual.

Transistor frequency response: General frequency considerations, low frequency response, Miller effect capacitance, high frequency response, multistage frequency effects.

Module-3

Multistage amplifiers: Cascade and cascode connections, Darlington circuits, analysis and design.

Feedback amplifiers: Feedback concept, different types, practical feedback circuits, analysis and design of feedback circuits.

Module-4

Power amplifiers: Amplifier types, analysis and design of different power amplifiers, distortion in power amplifiers.

Oscillators: Principle of operation, analysis and derivation of frequency of oscillation of phase shift oscillator, Wien bridge oscillator, RF and crystal oscillator and frequency stability.

Module-5

FETs: Construction, working and characteristics of JFET and MOSFET. Biasing of JFET and MOSFET, JFET and MOSFET amplifiers, analysis and design.

Table of Contents

Module-1

Diode circuits

Diode:

A pure silicon crystal or germanium crystal is known as an intrinsic semiconductor. There are not enough free electrons and holes in an intrinsic semi-conductor to produce a usable current. The electrical action of these can be modified by doping means adding impurity atoms to a crystal to increase either the number of free holes or no of free electrons.

When a crystal has been doped, it is called a extrinsic semi-conductor. They are of two types

- n-type semiconductor having free electrons as majority carriers
- p-type semiconductor having free holes as majority carriers

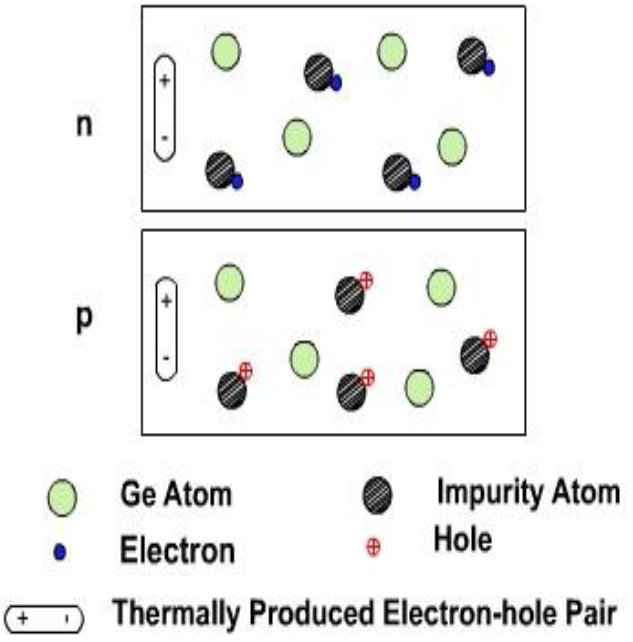
By themselves, these doped materials are of little use. However, if a junction is made by joining p-type semiconductor to n-type semiconductor a useful device is produced known as diode. It will allow current to flow through it only in one direction. The unidirectional properties of a diode allow current flow when forward biased and disallow current flow when reversed biased. This is called rectification process and therefore it is also called rectifier.

How is it possible that by properly joining two semiconductors each of which, by itself, will freely conduct the current in any direct refuses to allow conduction in one direction.

Consider first the condition of p-type and n-type germanium just prior to joining **fig. 1**. The majority and minority carriers are in constant motion.

The minority carriers are thermally produced and they exist only for short time after which they recombine and neutralize each other. In the mean time, other minority carriers have been produced and this process goes on and on.

The number of these electron hole pair that exist at any one time depends upon the temperature. The number of majority carriers is however, fixed depending on the number of impurity atoms available. While the electrons and holes are in motion but the atoms are fixed in place and do not move.



- Holes from the p-side diffuse into n-side where they recombine with free electrons.
- Free electrons from n-side diffuse into p-side where they recombine with free holes.
- The diffusion of electrons and holes is due to the fact that large no of electrons are concentrated in one area and large no of holes are concentrated in another area.
- When these electrons and holes begin to diffuse across the junction then they collide each other and negative charge in the electrons cancels the positive charge of the hole and both will lose their charges.
- The diffusion of holes and electrons is an electric current referred to as a recombination current. The recombination process decay exponentially with both time and distance from the junction. Thus most of the recombination occurs just after the junction is made and very near to junction.
- A measure of the rate of recombination is the lifetime defined as the time required for the density of carriers to decrease to 37% to the original concentration
- The impurity atoms are fixed in their individual places. The atoms itself is a part of the crystal and so cannot move. When the electrons and hole meet, their individual charge is cancelled and this leaves the originating impurity atoms with a net charge, the atom that produced the electron now lack an electronic and so becomes charged positively, whereas the atoms that produced the hole now lacks a positive charge and becomes negative.
- The electrically charged atoms are called ions since they are no longer neutral. These ions produce an electric field as shown in **fig. 3**. After several collisions occur, the electric field is great enough to repel rest of the majority carriers away of the junction. For example, an electron trying to diffuse from n to p side is repelled by the negative charge of the p-side. Thus diffusion process does not continue indefinitely but continues as long as the field is developed.
- This region is produced immediately surrounding the junction that has no majority carriers. The majority carriers have been repelled away from the junction and junction is depleted from

carriers. The junction is known as the barrier region or depletion region. The electric field represents a potential difference across the junction also called ***space charge potential or barrier potential .*** This potential is 0.7v for Si at 25^{o} celcious and 0.3v for Ge.

- The physical width of the depletion region depends on the doping level. If very heavy doping is used, the depletion region is physically thin because diffusion charge need not travel far across the junction before recombination takes place (short life time). If doping is light, then depletion is more wide (long life time).

The symbol of diode is shown in **fig. 4**. The terminal connected to p-layer is called anode (A) and the terminal connected to n-layer is called cathode (K)

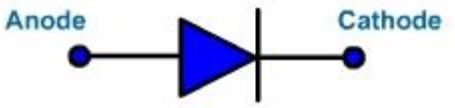
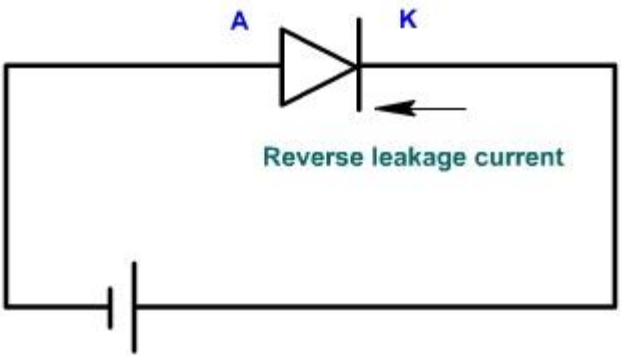


Fig.4

Reverse Bias:

If positive terminal of dc source is connected to cathode and negative terminal is connected to anode, the diode is called reverse biased as shown in **fig. 5**.



Space charge capacitance C_T of diode:

Reverse bias causes majority carriers to move away from the junction, thereby creating

more ions. Hence the thickness of depletion region increases. This region behaves as the dielectric material used for making capacitors. The p-type and n-type conducting on each side of dielectric act as the plate. The incremental capacitance C_T is defined by

$$C_T = \left|\frac{dQ}{dV}\right|$$

Since $i = \frac{dQ}{dt}$

Therefore, $i = C_T \frac{dV}{dt}$ **(E-1)**

where, dQ is the increase in charge caused by a change dV in voltage. C_T is not constant, it depends upon applied voltage, there fore it is defined as dQ / dV.

When p-n junction is forward biased, then also a capacitance is defined called *diffusion capacitance* C_D (rate of change of injected charge with voltage) to take into account the time delay in moving the charges across the junction by the diffusion process. It is considered as a fictitious element that allow us to predict time delay.

If the amount of charge to be moved across the junction is increased, the time delay is greater, it follows that diffusion capacitance varies directly with the magnitude of forward current.

$$C_D = \frac{dQ}{dV} = \frac{I\tau}{dV} \quad \textbf{(E-2)}$$

Relationship between Diode Current and Diode Voltage

An exponential relationship exists between the carrier density and applied potential of diode junction as given in equation E-3. This exponential relationship of the current i_D and the voltage v_D holds over a range of at least seven orders of magnitudes of current - that is a factor of 10^7.

$$i_D = I_0 \left[\exp\left(\frac{qv_D}{nkT}\right) - 1 \right] = I_0 \left[e^{\left(\frac{qv_D}{nkT}\right)} - 1 \right] \quad \textbf{(E-3)}$$

Where,

i_D= Current through the diode (dependent variable in this expression)
v_D= Potential difference across the diode terminals (independent variable in this expression)
I_O= Reverse saturation current (of the order of 10^{-15} A for small signal diodes, but I_O is a

strong function of temperature)
q = Electron charge: 1.60 x 10^{-19} joules/volt
k = Boltzmann's constant: 1.38 x $l0^{-23}$ joules /° K
T = Absolute temperature in degrees Kelvin (°K = 273 + temperature in °C)
n = Empirical scaling constant between 0.5 and 2, sometimes referred to as the Exponential Ideality Factor

The empirical constant, n, is a number that can vary according to the voltage and current levels. It depends on electron drift, diffusion, and carrier recombination in the depletion region. Among the quantities affecting the value of n are the diode manufacture, levels of doping and purity of materials. If n=1, the value of k T/ q is 26 mV at 25°C. When n=2, k T/ q becomes 52 mV.

For germanium diodes, n is usually considered to be close to 1. For silicon diodes, n is in the range of 1.3 to 1.6. n is assumed 1 for all junctions all throughout unless otherwise noted.

Equation **(E-3)** can be simplified by defining V_T =k T/q, yielding

$$i_D = I_O\left[\exp\left(\frac{v_D}{nV_T}\right) - 1\right] = I_O\left[e^{\left(\frac{v_D}{nV_T}\right)} - 1\right] \qquad \textbf{(E-4)}$$

At room temperature (25°C) with forward-bias voltage only the first term in the parentheses is dominant and the current is approximately given by

$$i_D = I_O\, e^{\frac{v_D}{nV_T}} \qquad \textbf{(E-5)}$$

The current-voltage (l-V) characteristic of the diode, as defined by (E-3) is illustrated in **fig. 1**. The curve in the figure consists of two exponential curves. However, the exponent values are such that for voltages and currents experienced in practical circuits, the curve sections are close to being straight lines. For voltages less than V_{ON}, the curve is approximated by a straight line of slope close to zero. Since the slope is the conductance (i.e., i / v), the conductance is very small in this region, and the equivalent resistance is very high. For voltages above V_{ON}, the curve is approximated by a straight line with a very large slope. The conductance is therefore very large, and the diode has a very small equivalent resistance.

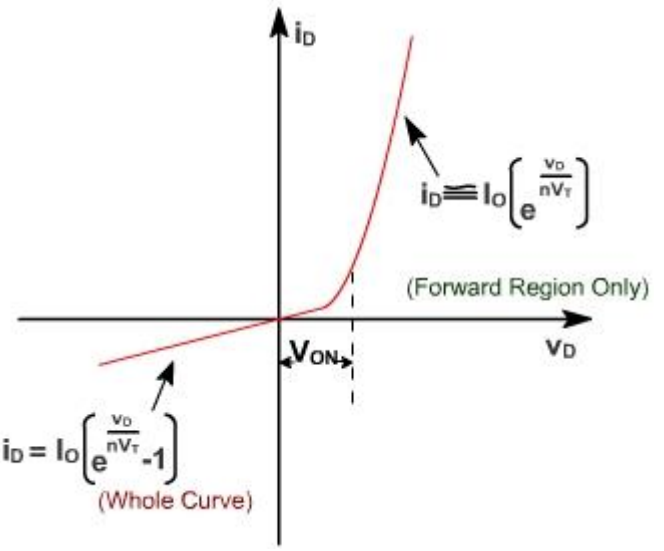


Fig.1 - Diode Voltage relationship

The slope of the curves of **fig.1** changes as the current and voltage change since the l-V characteristic follows the exponential relationship of relationship of equation (E-4). Differentiate the equation (E-4) to find the slope at any arbitrary value of $v_D$or i_D,

$$\frac{di_D}{dv_D} = \frac{I_O}{nV_T}\exp\left(\frac{v_D}{nV_T}\right) = \frac{I_O}{nV_T}e^{\frac{v_D}{nV_T}} \qquad \textbf{(E-6)}$$

This slope is the equivalent conductance of the diode at the specified values of v_D or i_D.

We can approximate the slope as a linear function of the diode current. To eliminate the exponential function, we substitute equation (E-4) into the exponential of equation (E-7) to obtain

$$\exp\left(\frac{v_D}{nV_T}\right) = \frac{i_D}{I_O} + 1 = \left(\frac{di_D}{dv_D}\right)\left(\frac{nV_T}{i_D}\right) \qquad \textbf{(E-7)}$$

A realistic assumption is that $I_O << i_D$ equation (E-7) then yields,

$$\frac{di_D}{dv_D} = \frac{i_D + I_O}{nV_T} \approx \frac{i_D}{nV_T} \qquad \textbf{(E-8)}$$

The approximation applies if the diode is forward biased. The dynamic resistance is the reciprocal of this expression.

$$r_d = \frac{nV_T}{i_D + I_0} \approx \frac{nV_T}{i_D} \qquad \textbf{(E-9)}$$

Although r_d is a function of i_d, we can approximate it as a constant if the variation of i_D is small. This corresponds to approximating the exponential function as a straight line within a specific operating range.

Normally, the term R_f to denote diode forward resistance. R_f is composed of r_d and the contact resistance. The contact resistance is a relatively small resistance composed of the resistance of the actual connection to the diode and the resistance of the semiconductor prior to the junction. The reverse-bias resistance is extremely large and is often approximated as infinity.

Temperature Effects:

Temperature plays an important role in determining the characteristic of diodes. As temperature increases, the turn-on voltage, v_{ON}, decreases. Alternatively, a decrease in temperature results in an increase in v_{ON}. This is illustrated in **fig. 2,** where V_{ON} varies linearly with temperature which is evidenced by the evenly spaced curves for increasing temperature in 25 °C increments.

The temperature relationship is described by equation

$$V_{ON}(T_{New}) - V_{ON}(T_{room}) = k_T(T_{New} - T_{room}) \qquad \textbf{(E-10)}$$

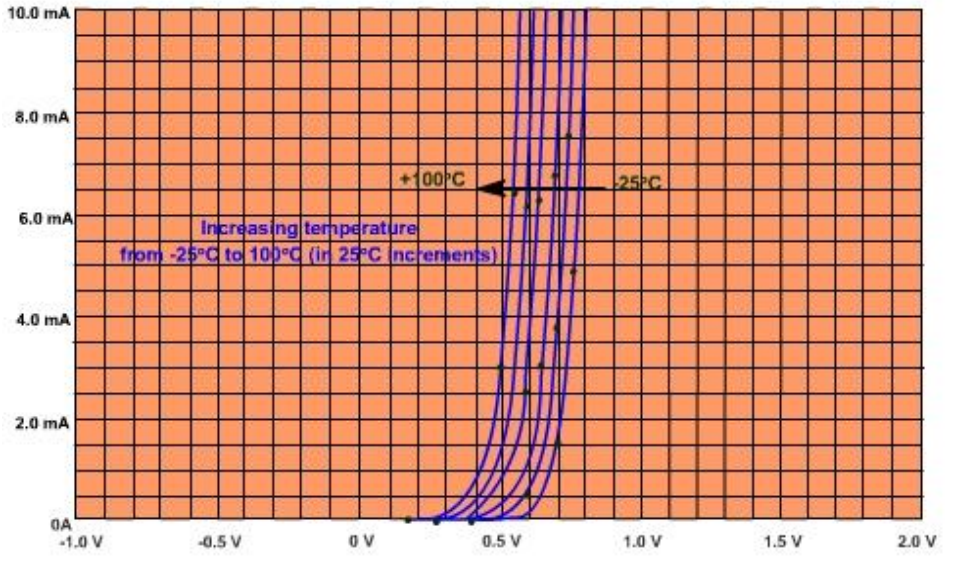


Fig. 2 - Dependence of iD on temperature versus vD for real diode (kT = -2.0 mV /°C)

where,

T_{room}= room temperature, or 25°C.
T_{New}= new temperature of diode in °C.
$V_{ON}(T_{room})$ = diode voltage at room temperature.
$V_{ON}(T_{New})$ = diode voltage at new temperature.
k_T = temperature coefficient in V/°C.

Although k_T varies with changing operating parameters, standard engineering practice permits approximation as a constant. Values of k_T for the various types of diodes at room temperature are given as follows:

k_T= -2.5 mV/°C for germanium diodes
k_T = -2.0 mV/°C for silicon diodes

The reverse saturation current, I_O also depends on temperature. At room temperature, it increases approximately 16% per °C for silicon and 10% per °C for germanium diodes. In other words, I_O approximately doubles for every 5 °C increase in temperature for silicon, and for every 7 °C for germanium. The expression for the reverse saturation current as a function of temperature can be approximated as

$$I_0(atT_2) = I_0(atT_1)\exp(k_i(T_2 - T_1)) = I_0(atT_1)e^{K_i(T_2-T_1)} \quad \textbf{(E-11)}$$

where K_i= 0.15/°C (for silicon) and T1 and T2 are two arbitrary temperatures.

Diode Operating Point

Example - 1:

When a silicon diode is conducting at a temperature of 25°C, a 0.7 V drop exists across its terminals. What is the voltage, V_{ON}, across the diode at 100°C?

Solution:

The temperature relationship is described by

$V_{ON}(T_{New})$? $V_{ON}(T_{room}) = K_T (T_{New}$? $T_{room})$

or, $V_{ON}(T_{New}) = V_{ON}(T_{room}) + K_T (T_{new}$? $T_{room})$

Given $V_{ON}(T_{room}) = 0{,}7$ V, T_{room}= 25° C, T_{New}= 100° C

Therefore, $V_{ON}(T_{New}) = 0.7 + (-2 \times 10^{-3})(100-75) = 0.55$ V

Example - 2:

Find the output current for the circuit shown in **fig.1(a).**

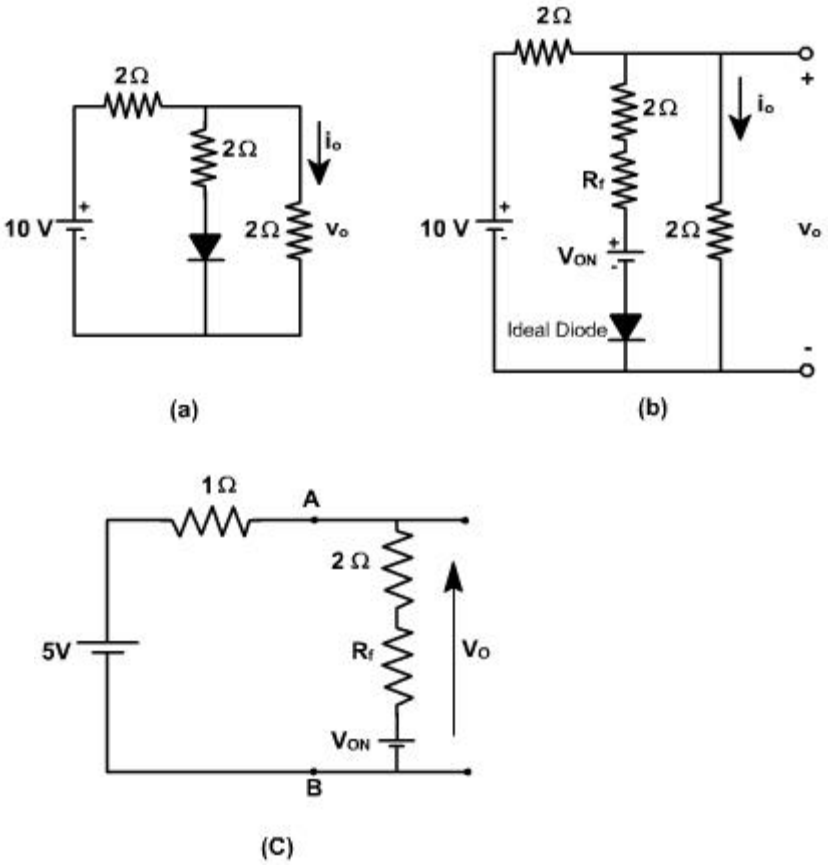


Fig.1- Circuit for Example 2

Solutions:

Since the problem contains only a dc source, we use the diode equivalent circuit, as shown in **fig. 1(b).** Once we determine the state of the ideal diode in this model (i.e., either open circuit or short circuit), the problem becomes one of simple dc circuit analysis.

It is reasonable to assume that the diode is forward biased. This is true since the only external source is 10 V, which clearly exceeds the turn-on voltage of the diode, even taking the voltage division into account. The equivalent circuit then becomes that of **fig. 1(b).** with the diode replaced by a short circuit.

The Thevenin's equivalent of the circuit between A and B is given by **fig. 1(c).**

The output voltage is given by

$$v_o = \left(\frac{5 - V_{ON}}{3 + R_f}\right)(2 + R_f) + V_{ON}$$

or, $$v_o = \frac{10 + V_{ON} + 5R_f}{3 + R_f}$$

If V_{ON}= 0.7V, and R_f= 0.2 W , then

V_o = 3.66V

Diode Operating Point

Example - 3

The circuit of <u>fig. 2</u>, has a source voltage of Vs = 1.1 + 0.1 sin 1000t. Find the current, iD. Assume that

nVT = 40 mV

VON = 0.7 V

Solution:

We use KVL for dc equation to yield

$V_s = V_{ON} + I_D R_L$

$$I_D = \frac{V_S - V_{ON}}{R_L} = 4 \text{ mA}$$

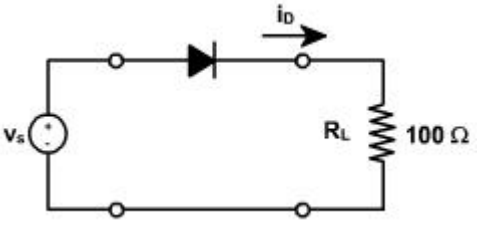


Fig.2

This sets the dc operating point of the diode. We need to determine the dynamic resistance so we can establish the resistance of the forward-biased junction for the ac signal.

$$r_D = \frac{nV_T}{I_D} = 10\ \Omega$$

Assuming that the contact resistance is negligible Rf= rD Now we can replace the forward-biased diode with a 10 W resistor. Again using KVL, we have,

vs= Rf id + RL id

$$i_d = \frac{v_S}{R_f + R_L} = 0.91 \sin 1000\,t \quad mA$$

The diode current is given by

I = 4 + 0.91 sin 1000 t mA

Since iD is always positive, the diode is always forward-biased, and the solution is complete.

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Diode Operating Point

Small Signal Operation of Real diode:

Consider the diode circuit shown in **fig. 3**.

$V = V_D + I_d R_L$

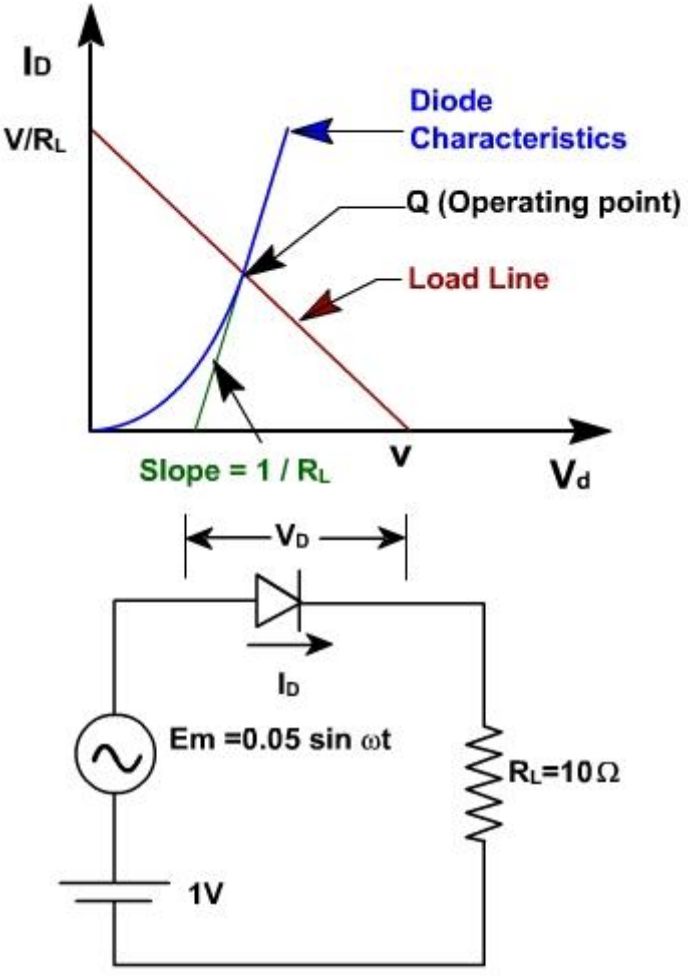
$V_D = V - I_d R_L$

This equation involves two unknowns and cannot be solved. The straight line represented by the above equation is known as the **load line**. The load line passes through two points,

$I = 0, V_D = V$

and $V_D = 0, I = V / R_L$.

The slope of this line is equal to 1/ RL. The other equation in terms of these two variables VD & Id, is given by the static characteristic. The point of intersection of straight line and diode characteristic gives the operating point as shown in fig. 4.



ohm.

The resulting input voltage is the sum of dc voltage and sinusoidal ac voltage. Therefore, as the diode voltage varies, diode current also varies, sinusoidally. The intersection of load line and diode characteristic for different input voltages gives the output voltage as shown in fig. 6.

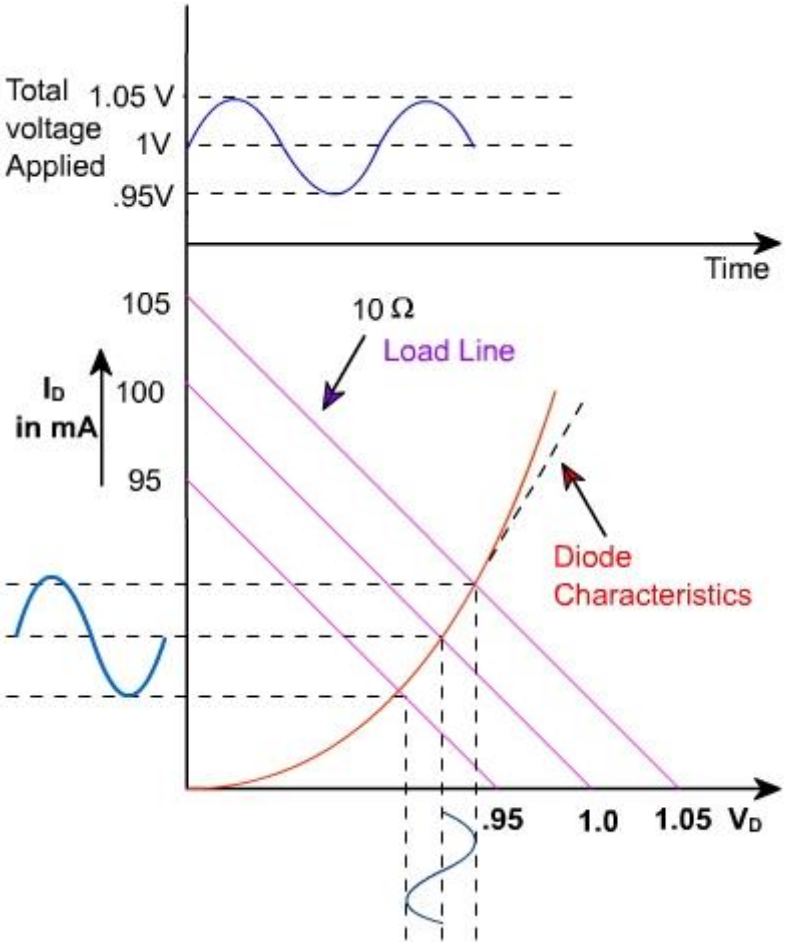
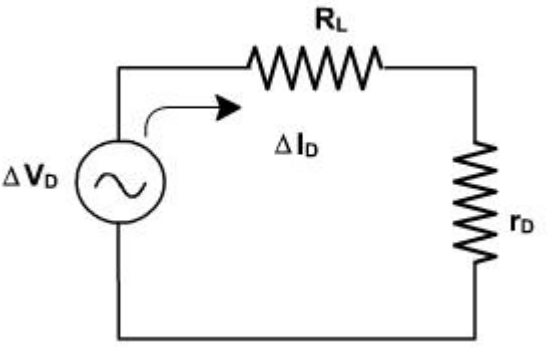


Fig. 6

In certain applications only ac equivalent circuit is required. Since only ac response of the circuit is considered DC Source is not shown in the equivalent circuit of fig. 7. The resistance rf represents the dynamic resistance or ac resistance of the diode. It is obtained by taking the ratio of Δ VD/ Δ ID at operating point.

Dynamic Resistance Δ rD = Δ VD / Δ ID

Let us consider a circuit shown in fig. 5 having dc voltage and sinusoidal ac voltage. Say



V = 1V, RL=10

Fig. 7

<u>Applications of Diode</u>

Diode Approximation: (Large signal operations):

1. Ideal Diode:

- **When diode is forward biased, resistance offered is zero,**
- **When it is reverse biased resistance offered is infinity. It acts as a perfect switch.**

The characteristic and the equivalent circuit of the diode is shown in <u>fig. 1.</u>

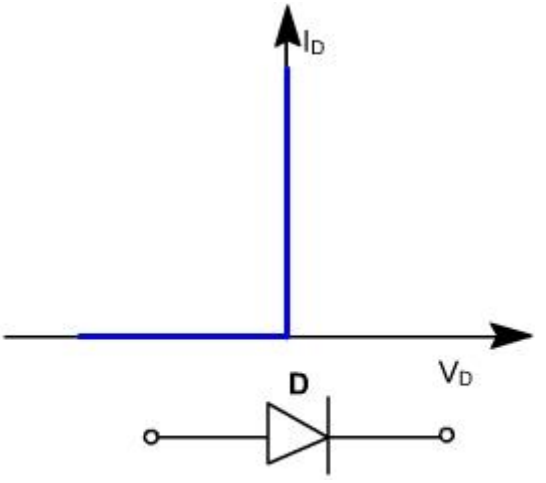


Fig. 1

2. Second Approximation:

- **When forward voltage is more than 0.7 V, for Si diode then it conducts and offers zero resistance. The drop across the diode is 0.7V.**
- **When reverse biased it offers infinite resistance.**

The characteristic and the equivalent circuit is shown in fig. 2.

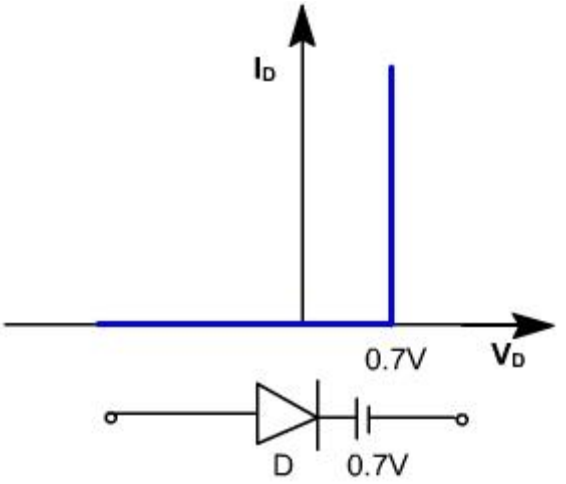


Fig. 2

3. 3rd Approximation:

- **When forward voltage is more than 0.7 V, then the diode conducts and the voltage drop across the diode becomes 0.7 V and it offers resistance Rf (slope of the current)**

VD= 0.7 + ID Rf.

The output characteristic and the equivalent circuit is shown in fig. 3.

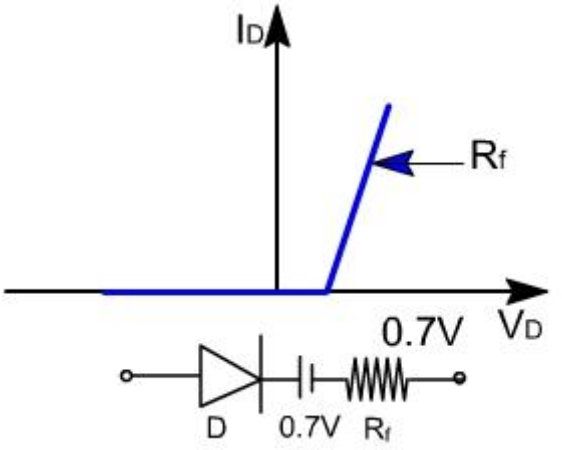


Fig. 3

- **When reverse biased resistance offered is very high & not infinity, then the diode equivalent circuit is as shown in fig. 4.**

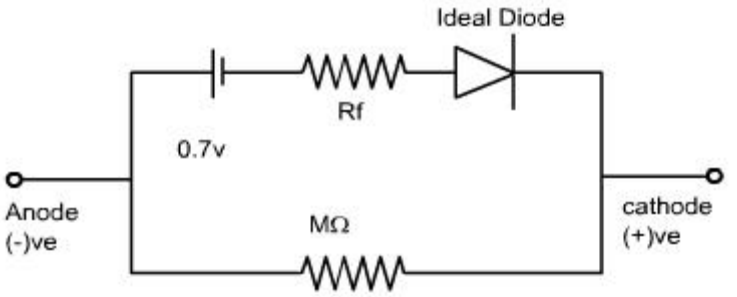


Fig. 4

Example - 1:

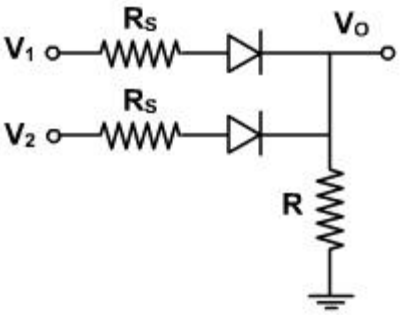
Calculate the voltage output of the circuit shown in **fig. 5** for following inputs

(a) $V_1 = V_2 = 0$.

(b) $V_1 = V$, $V_2 = 0$.

(c) $V_1 = V_2 = V$ knew voltage = V_r

Forward resistance of each diode is R_f.



Solution:

(a). When both V_1 and V_2 are zero , then the diodes are unbiased. Therefore,

$V_o = 0$ V

(b). When $V_1 = V$ and $V_2 = 0$, then one upper diode is forward biased and lower diode is unbiased. The resultant circuit using third approximation of diode will be as shown in **fig. 6**.

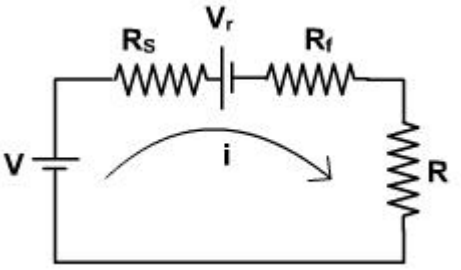


Fig. 6

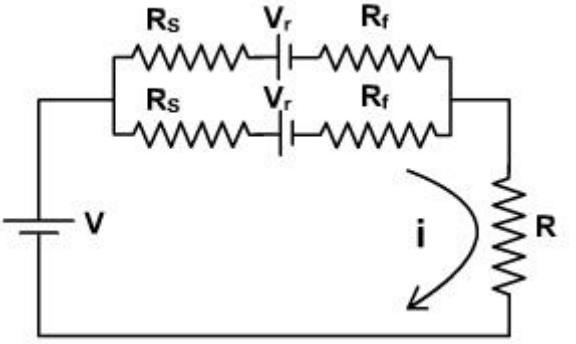


Fig. 7

Applying KVL, we get

$$V = I(R_f + R_s + R) + V_r$$

$$\therefore I = \frac{V - Vr}{R_s - R_f + R}$$

(c) When both V_1 and V_2 are same as V, then both the diodes are forward biased and conduct. The resultant circuit using third approximation of diode will be as shown in **Fig. 7**.

$$V = \frac{1}{2}(R_f + R_s) + V_r + 1$$

$$I = \frac{V - V_r}{\left(\frac{R_s + R_f}{2} + R\right)}$$

Half wave Rectifier:

The single ? phase half wave rectifier is shown in **fig. 8**.

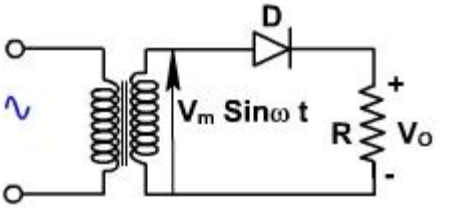


Fig. 8

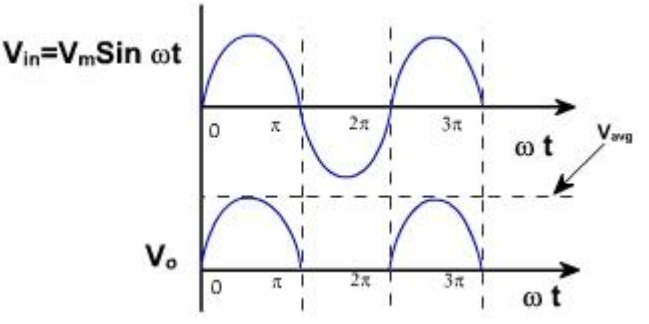


Fig. 9

In positive half cycle, D is forward biased and conducts. Thus the output voltage is same as the input voltage. In the negative half cycle, D is reverse biased, and therefore output voltage is zero. The output voltage waveform is shown in **fig. 9**.

The average output voltage of the rectifier is given by

$$V_{avg} = \frac{1}{2}\int_0^{\pi} V_m \sin \omega t \, d(\omega t)$$
$$= \frac{V_m}{\pi} = 0.318 V_m$$

The average output current is given by

$$I_{avg} = \frac{V_m}{\pi R}$$

When the diode is reverse biased, entire transformer voltage appears across the diode. The maximum voltage across the diode is V_m. The diode must be capable to withstand this voltage. Therefore PIV half wave rating of diode should be equal to V_m in case of single-phase rectifiers. The average current rating must be greater than I_{avg}

Full Wave Rectifier:

A single ? phase full wave rectifier using center tap transformer is shown in **fig. 10.** It supplies current in both half cycles of the input voltage.

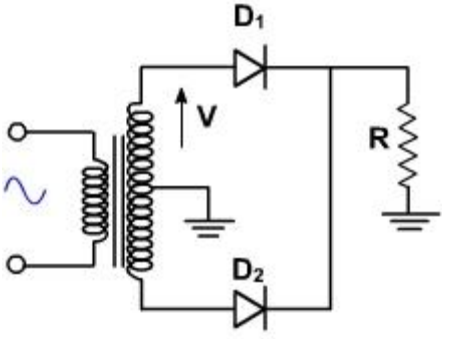


Fig. 10

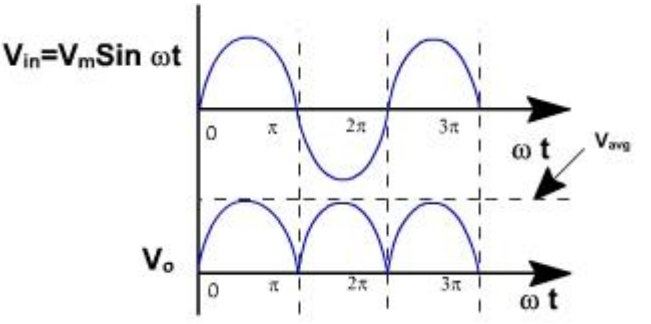


Fig. 11

In the first half cycle D_1 is forward biased and conducts. But D_2 is reverse biased and does not conduct. In the second half cycle D_2 is forward biased, and conducts and D_1 is reverse biased. It is also called 2 ? pulse midpoint converter because it supplies current in both the half cycles. The output voltage waveform is shown in **fig. 11**.

The average output voltage is given by

$$V_{avg} = \frac{1}{\pi}\int_0^{\pi} V_m \sin\omega t \, d(\omega t)$$
$$= \frac{2V_m}{\pi}$$

and the average load current is given by

$$I_{avg} = \frac{2V_m}{\pi R}$$

When D_1 conducts, then full secondary voltage appears across D_2, therefore PIV rating of the diode should be 2 V_m.

Bridge Rectifier:

The single ? phase full wave bridge rectifier is shown in **fig. 1.** It is the most widely used rectifier. It also provides currents in both the half cycle of input supply.

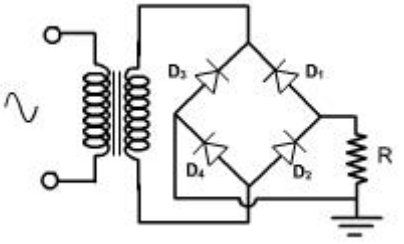


Fig. 1

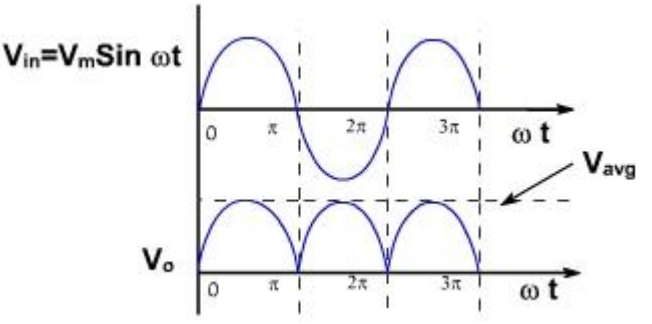


Fig. 2

In the positive half cycle, D_1 & D_4 are forward biased and D_2 & D_3 are reverse biased. In the negative half cycle, D_2 & D_3 are forward biased, and D_1 & D_4 are reverse biased. The output voltage waveform is shown in **fig. 2** and it is same as full wave rectifier but the advantage is that PIV rating of diodes are V m and only single secondary transformer is required.

The main disadvantage is that it requires four diodes. When low dc voltage is required then secondary voltage is low and diodes drop (1.4V) becomes significant. For low dc output, 2-pulse center tap rectifier is used because only one diode drop is there.

The ripple factor is the measure of the purity of dc output of a rectifier and is defined as

$$\text{Ripple factor} = \frac{\text{r.m.s value of the ac output voltage}}{\text{average dc output voltage}}$$
$$= \sqrt{V_0^2 + \sum_{n=1}^{\infty} V_n^2}$$

Therefore,

$$\text{Ripple factor} = \frac{\sqrt{V_{rms}^2 - V_o^2}}{V_o}$$

$$= \sqrt{\left(\frac{V_{rms}}{V_o}\right)^2 - 1}$$

Clippers:

Clipping circuits are used to select that portion of the input wave which lies above or below some reference level. Some of the clipper circuits are discussed here. The transfer characteristic (v_o vs v_i) and the output voltage waveform for a given input voltage are also discussed.

Clipper Circuit 1:

The circuit shown in **fig. 3**, clips the input signal above a reference voltage (V_R).

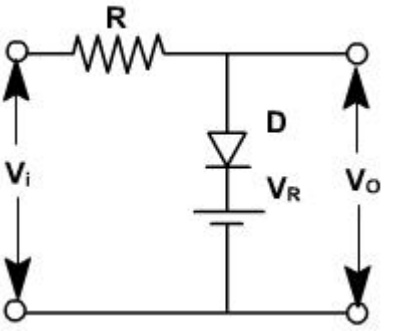


Fig. 3

In this clipper circuit,

If $v_i < V_R$, diode is reversed biased and does not conduct. Therefore, $v_o = v_i$

and, if $v_i > V_R$, diode is forward biased and thus, $v_o = V_R$.

The transfer characteristic of the clippers is shown in **fig. 4**.

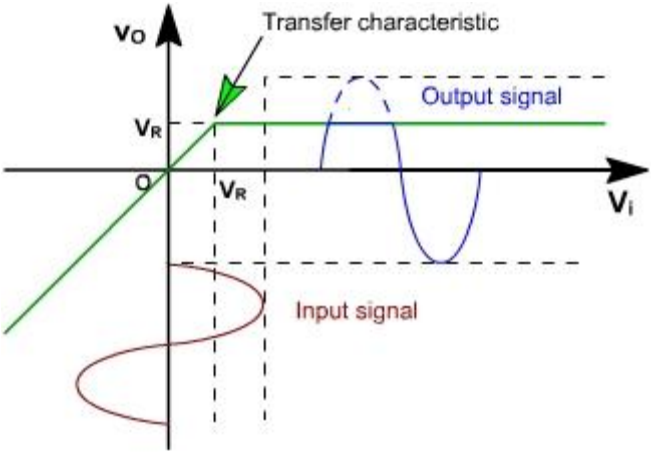


Fig. 4

Clipper Circuit 2:

The clipper circuit shown in **fig. 5** clips the input signal below reference voltage V_R.

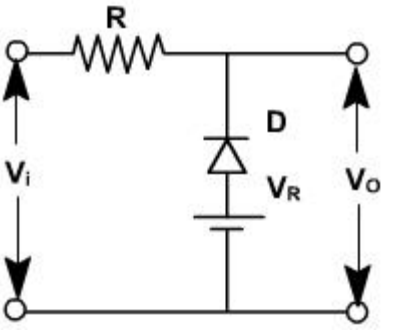


Fig. 5

In this clipper circuit,

If $v_i > V_R$, diode is reverse biased. $v_o = v_i$

and, If $v_i < V_R$, diode is forward biased. $v_o = V_R$

The transfer characteristic of the circuit is shown in **fig. 6**.

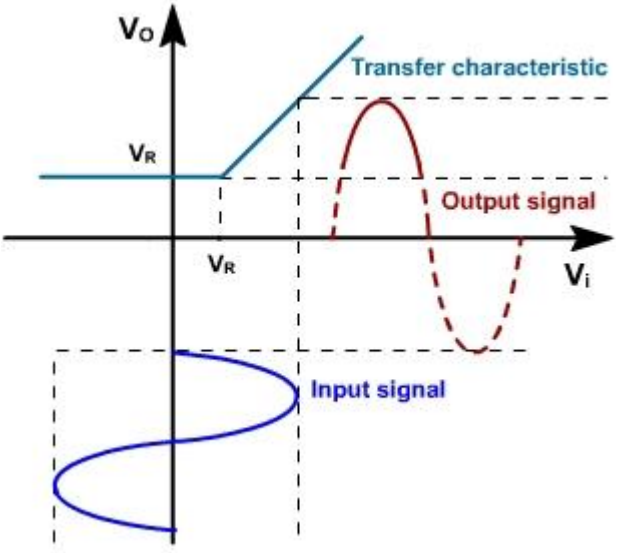


Fig. 6

Clipper Circuit 3: To clip the input signal between two independent levels ($V_{R1} < V_{R2}$), the clipper circuit is shown in **fig. 7**.

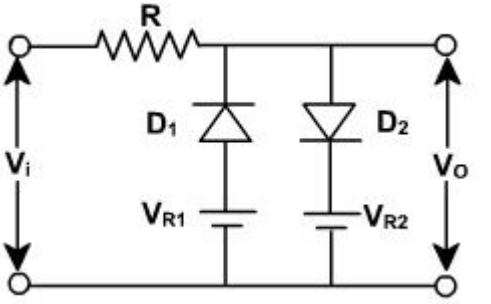


Fig. 7

The diodes D_1 & D_2 are assumed ideal diodes.

For this clipper circuit, when $v_i \leq V_{R1}$, $v_o = V_{R1}$

and, $v_i \geq V_{R2}$, $v_o = V_{R2}$

and, $V_{R1} < v_i < V_{R2}$ $v_o = v_i$

The transfer characteristic of the clipper is shown in **fig. 8.**

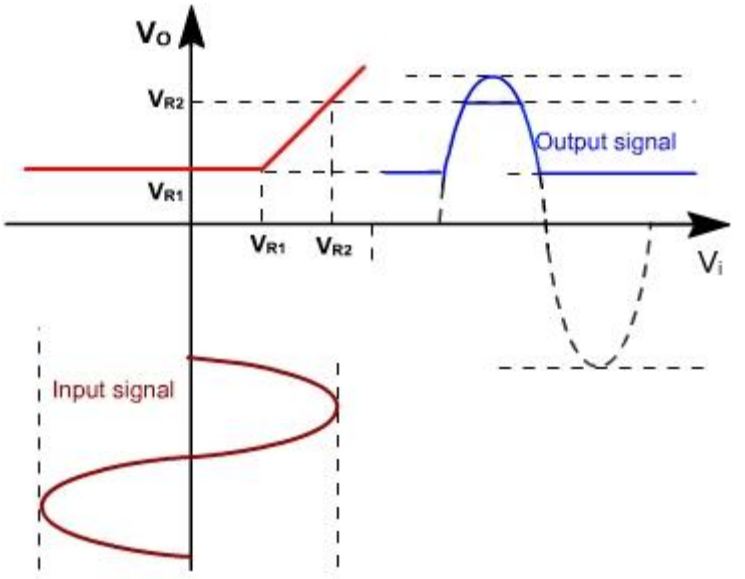


Fig. 8

Clippers:

Clipping circuits are used to select that portion of the input wave which lies above or below some reference level. Some of the clipper circuits are discussed here. The transfer characteristic (v_o vs v_i) and the output voltage waveform for a given input voltage are also discussed.

Clipper Circuit 1:

The circuit shown in **fig. 3**, clips the input signal above a reference voltage (V_R).

In this clipper circuit,

If $v_i < V_R$, diode is reversed biased and does not conduct. Therefore, $v_o = v_i$

and, if $v_i > V_R$, diode is forward biased and thus, $v_o = V_R$.

The transfer characteristic of the clippers is shown in **fig. 4.**

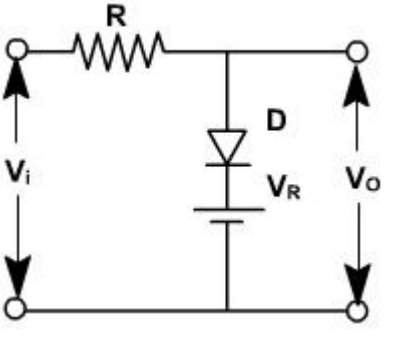


Fig. 3

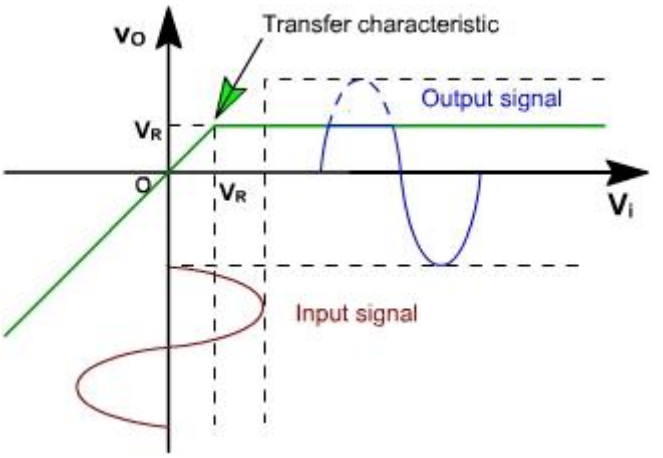


Fig. 4

Clipper Circuit 2:

The clipper circuit shown in **fig. 5** clips the input signal below reference voltage V_R.

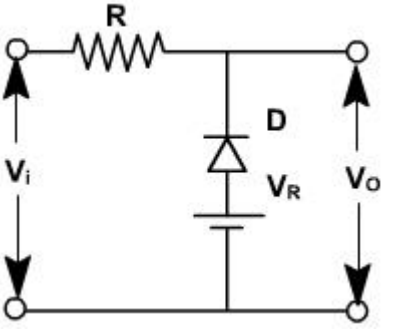


Fig. 5

In this clipper circuit,

If $v_i > V_R$, diode is reverse biased. $v_o = v_i$

and, If $v_i < V_R$, diode is forward biased. $v_o = V_R$

The transfer characteristic of the circuit is shown in **fig. 6**.

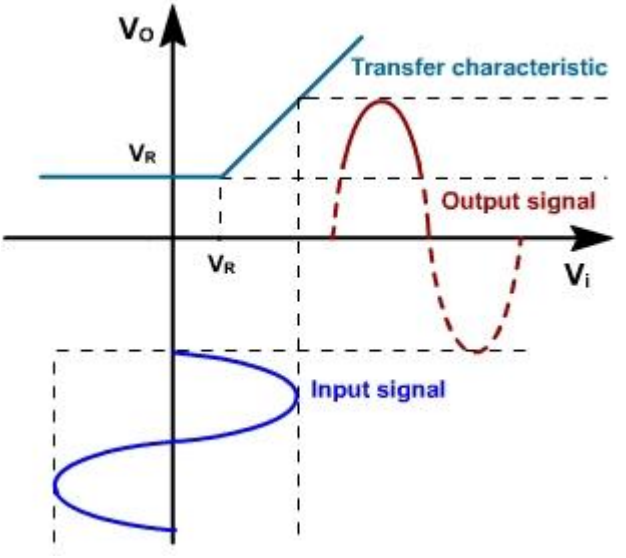


Fig. 6

Clipper Circuit 3:

To clip the input signal between two independent levels ($V_{R1} < V_{R2}$), the clipper circuit is shown in **fig. 7.**

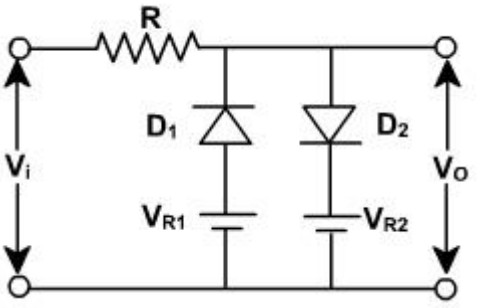


Fig. 7

The diodes D_1 & D_2 are assumed ideal diodes.

For this clipper circuit, when $v_i \leq V_{R1}$, $v_o = V_{R1}$

and, $v_i \geq V_{R2}$, $v_o = V_{R2}$

and, $V_{R1} < v_i < V_{R2}$ $v_o = v_i$

The transfer characteristic of the clipper is shown in **fig. 8.**

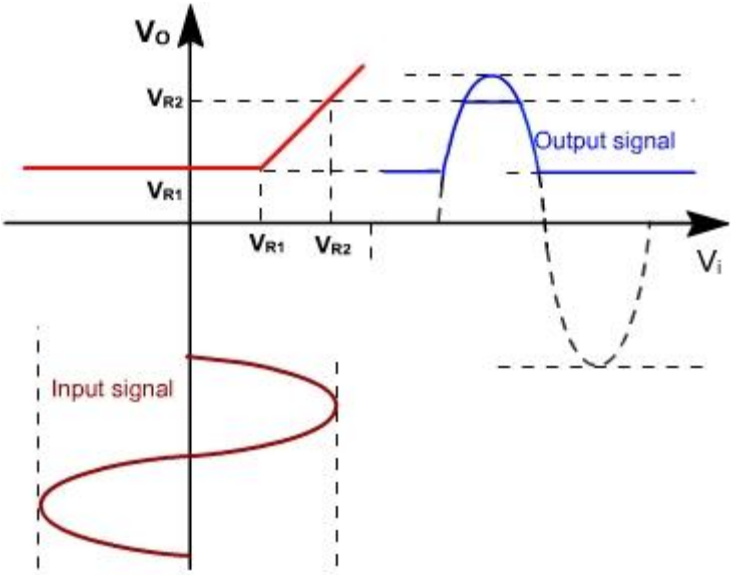


Fig. 8

Example - 1:

Find the output voltage v out of the clipper circuit of **fig. 7(a)** assuming that the diodes are

a. ideal.
b. $V_{on} = 0.7$ V. For both cases, assume R_F is zero.

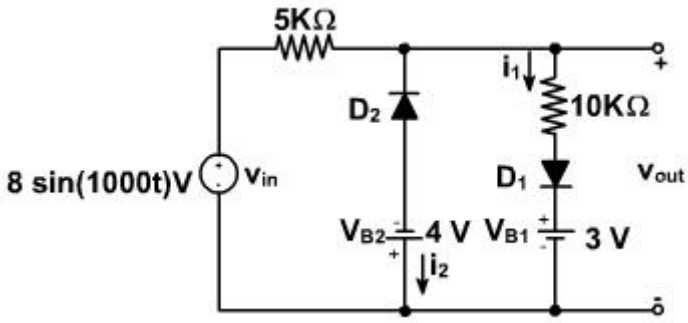


Fig. 7(a)

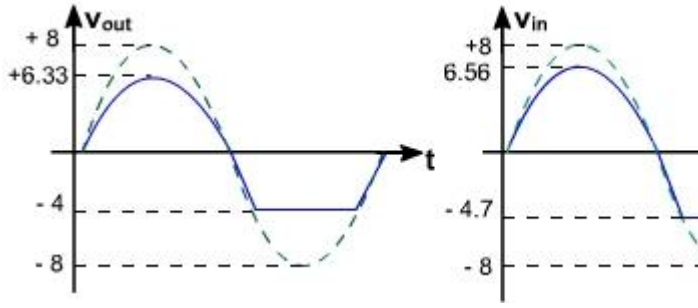


Fig. 7(b)

Solution:

(a). When $v_{in}$is positive and $v_{in} < 3$, then $v_{out} = v_{in}$

and when v_{in} is positive and $v_{in} > 3$, then

$$i_1 = \frac{v_{in} - 3}{1.5 \times 10^4}$$

$$v_{out} = 10^4 i_1 + 3 = \frac{2}{3} v_{in} + 1$$

At v_{in} = 8 V(peak), v_{out} = 6.33 V.

When $v_{in}$is negative and $v_{in} > -4$, then $v_{out} = v_{in}$

When v_{in} is negative and $v_{in} < -4$, then $v_{out} = -4V$

The resulting output wave shape is shown in **fig. 7(b)**.

(b). When V_{ON} = 0.7 V, v_{in} is positive and $v_{in} < 3.7$ V, then $v_{out} = v_{in}$

When $v_{in} > 3.7$ V, then

$$i_1 = \frac{v_{in} - 3.7}{1.5 \times 10^4}$$

$$v_{out} = 10^4 i_1 + 3.7 = \frac{2}{3} v_{in} + 1.23$$

When v_{in} = 8V, v_{out} = 6.56 V.

When v_{in} is negative and $v_{in} > -4.7$ V, then $v_{out} = v_{in}$

When $v_{in} < -4.7$ V, then $v_{out} = -4.7$ V

The resulting output wave form is shown in **fig. 7(b)**.

Clamper Circuits:

Clamping is a process of introducing a dc level into a signal. For example, if the input voltage swings from -10 V and +10 V, a positive dc clamper, which introduces +10 V in the input will produce the output that swings ideally from 0 V to +20 V. The complete waveform is lifted up by +10 V.

Negative Diode clamper:

A negative diode clamper is shown in **fig. 8**, which introduces a negative dc voltage equal to peak value of input in the input signal.

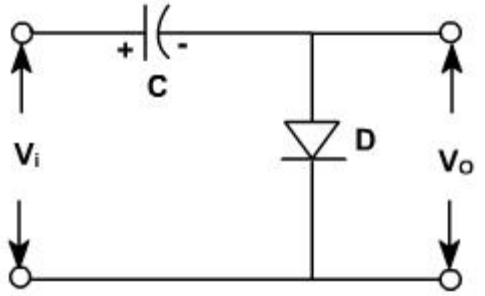


Fig. 8

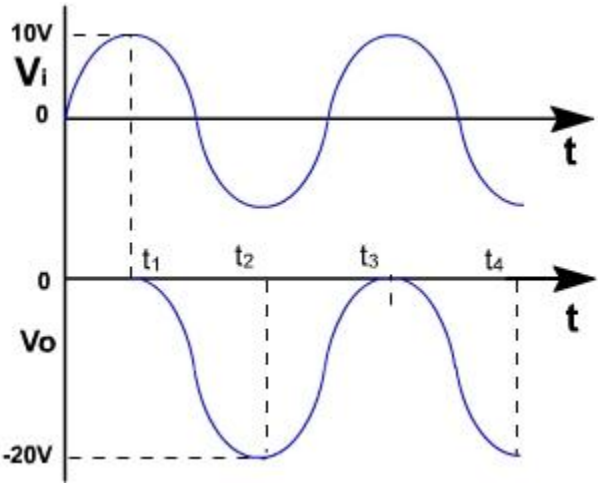


Fig. 9

Let the input signal swings form +10 V to -10 V. During first positive half cycle as V i rises from 0 to 10 V, the diode conducts. Assuming an ideal diode, its voltage, which is also the output must be zero during the time from 0 to t_1. The capacitor charges during this period to 10 V, with the polarity shown.

At that V_i starts to drop which means the anode of D is negative relative to cathode, ($V_D = v_i - v_c$) thus reverse biasing the diode and preventing the capacitor from discharging. **Fig. 9**. Since the capacitor is holding its charge it behaves as a DC voltage source while the diode appears as an open circuit, therefore the equivalent circuit

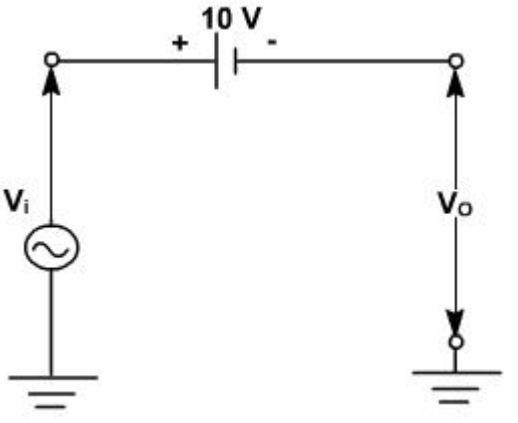


Fig. 10

becomes an input supply in series with -10 V dc voltage as shown in **fig. 10**, and the resultant output voltage is the sum of instantaneous input voltage and dc voltage (-10 V).

Positive Clamper:

The positive clamper circuit is shown in **fig. 1**, which introduces positive dc voltage equal to the peak of input signal. The operation of the circuit is same as of negative clamper.

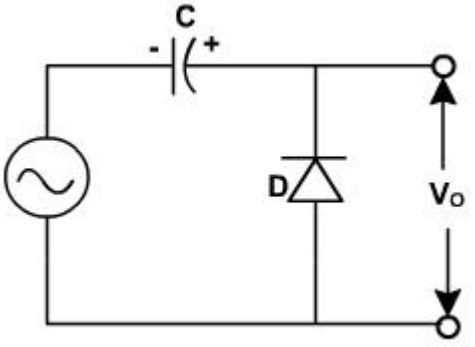


Fig. 1

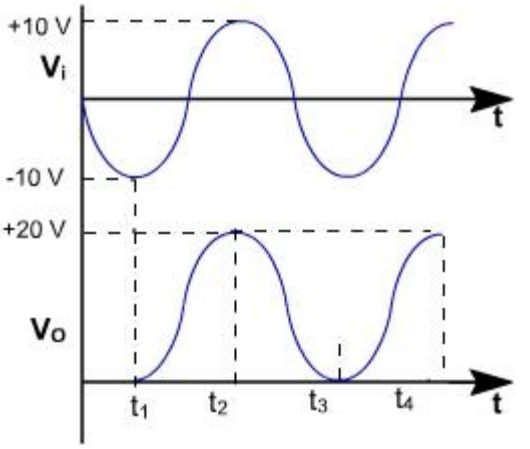


Fig. 2

Let the input signal swings form +10 V to -10 V. During first negative half cycle as V_i rises from 0 to -10 V, the diode conducts. Assuming an ideal diode, its voltage, which is also the output must be zero during the time from 0 to t_1. The capacitor charges during this period to 10 V, with the polarity shown.

After that V_i starts to drop which means the anode of D is negative relative to cathode, ($V_D = v_i - v_C$) thus reverse biasing the diode and preventing the capacitor from discharging. **Fig. 2.** Since the capacitor is holding its charge it behaves as a DC voltage source while the diode appears as an open circuit, therefore the equivalent circuit becomes an input supply in series with +10 V dc voltage and the resultant output voltage is the sum of instantaneous input voltage and dc voltage (+10 V).

To clamp the input signal by a voltage other than peak value, a dc source is required. As shown in **fig. 3**, the dc source is reverse biasing the diode.

The input voltage swings from +10 V to -10 V. In the negative half cycle when the voltage exceed 5V then D conduct. During input voltage variation from ?5 V to -10 V, the capacitor charges to

5 V with the polarity shown in **fig. 3**. After that D becomes reverse biased and open circuited. Then complete ac signal is shifted upward by 5 V. The output waveform is shown in **fig. 4.**

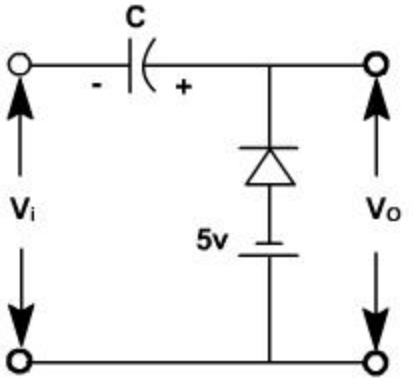


Fig. 3

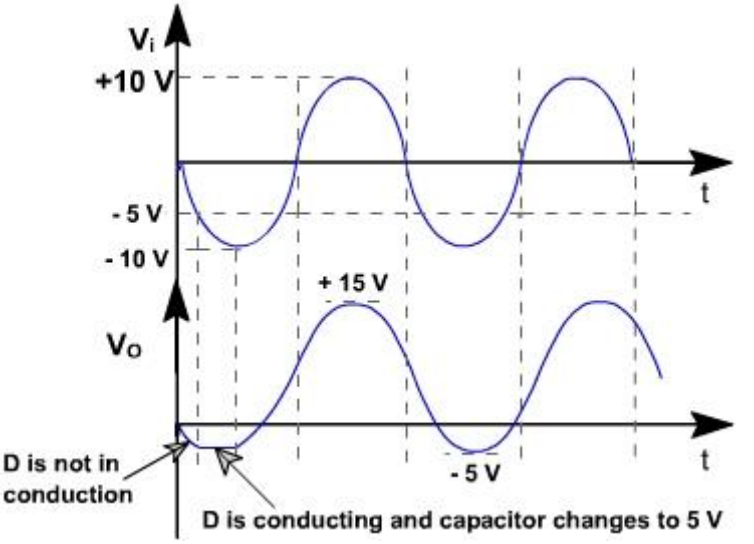


Fig. 4

Voltage Doubler :

A voltage doubler circuit is shown in **fig. 5**. The circuit produces a dc voltage, which is double the peak input voltage.

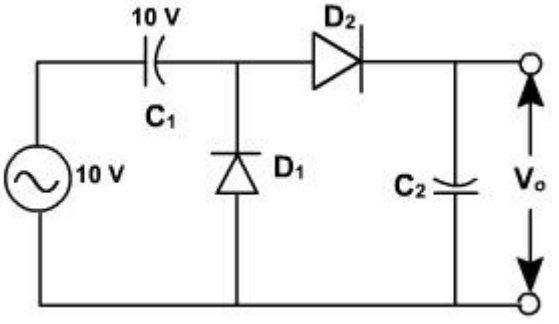


Fig. 5

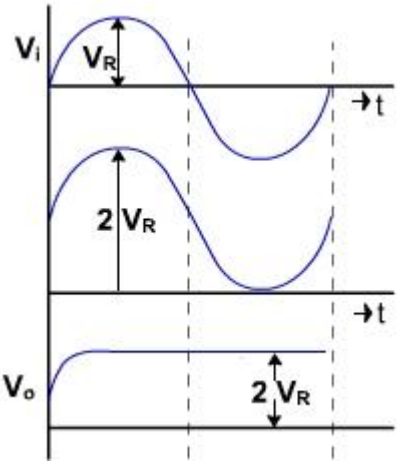


Fig. 6

At the peak of the negative half cycle D_1 is forward based, and D_2 is reverse based. This charges C_1 to the peak voltage V_p with the polarity shown. At the peak of the positive half cycle D_1 is reverse biased and D_2 is forward biased. Because the source and C_1 are in series, C_2 will change toward $2V_p$. e.g. Capacitor voltage increases continuously and finally becomes 20V. The voltage waveform is shown in **fig. 6**.

To understand the circuit operation, let the input voltage varies from -10 V to +10 V. The different stages of circuit from 0 to t_{10} are shown in **fig. 7(a)**.

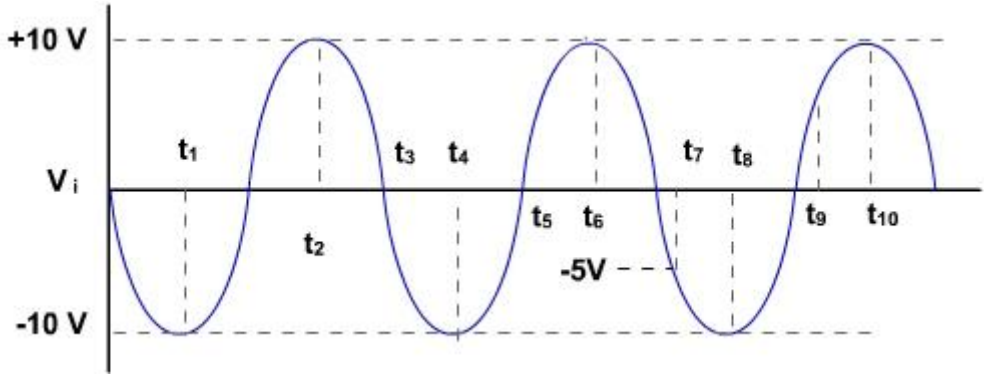


Fig. 7(a)

During 0 to t_1, the input voltage is negative, D_1 is forward biased the capacitor is charged to ?10 V with the polarity as shown in **fig. 7b**.

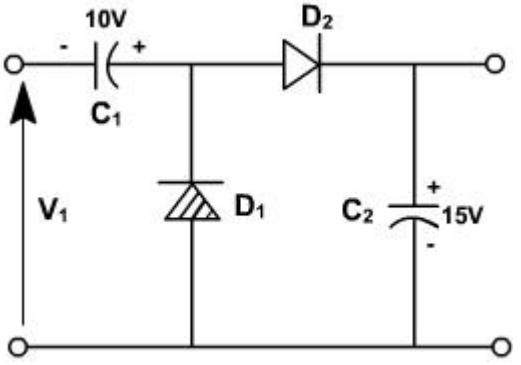


Fig. 7(b)

During t_1 to t_2, D_2 becomes forward biased and conducts and at t_2, when V_i is 10V total voltage change is 20V. If $C_1 = C_2 = C$, both the capacitor voltages charge to +10 V i.e. C_1 voltage becomes 0 and C_2 charges to +10V.

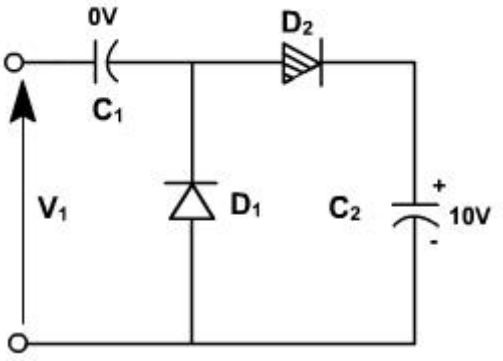


Fig. 7(c)

From t_2 to t_3 there is no conduction as both D_1 and D_2 are reverse biased. During t_3 to t_4 D_1 is forward biased and conducts. C_1 again charges to +10V

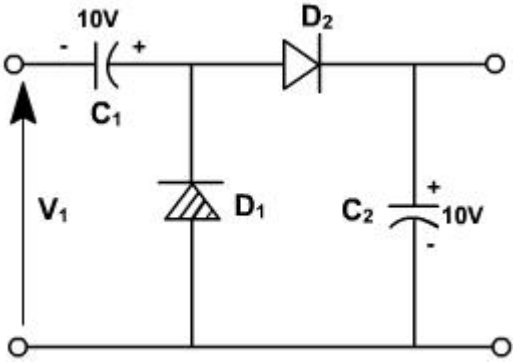


Fig. 7(d)

During t_4 to t_5 both D_1 and D_2 are reverse biased and do not conduct. During t_5 to t_6 D_2 is forward biased and conducts. The capacitor C_2 voltage becomes +15 V and C_1 voltage becomes +5 V.

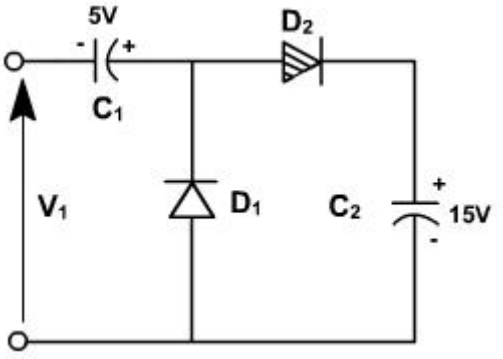


Fig. 7(e)

Again during t_6 to t_7 there is no conduction and during t_7 to t_8, D_1 conducts. The capacitor C_1 recharges to 10 V.

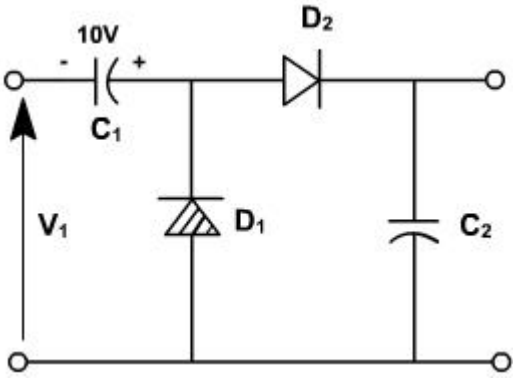


Fig. 7(f)

During t_8 to t_9 both D_1 and D_2 are reverse biased and there is no conduction. During t_9 to t_{10} D_2 conducts and capacitor C_2 voltage becomes + 17.5 V and C_1 voltage becomes 7.5V. This process continues till the capacitor C_1 voltage becomes +20V.

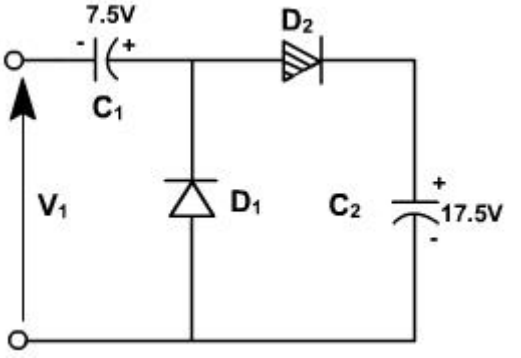


Fig. 7(g)

The power handling capacity of these diodes is better. The power dissipation of a zener diode equals the product of its voltage and current.

$P_Z = V_Z I_Z$

The amount of power which the zener diode can withstand ($V_Z.I_{Z(max)}$) is a limiting factor in power supply design.

Transistor biasing

To Understand :

- Concept of Operating point and stability
- Analyzing Various biasing circuits and their comparison with respect to stability

BJT – A Review

- Invented in 1948 by Bardeen, Brattain and Shockley
- Contains three adjoining, alternately doped semiconductor regions: Emitter (E), Base (B), and Collector (C)
- The middle region, base, is very thin
- Emitter is heavily doped compared to collector. So, emitter and collector are not interchangeable.

Three operating regions

- **Linear** – **region** operation:
  - Base – emitter junction forward biased
- Base – collector junction reverse biased
- **Cutoff** – **region** operation:
- Base – emitter junction reverse biased
- Base – collector junction reverse biased
- **Saturation** – **region** operation:
- Base – emitter junction forward biased
- Base – collector junction forward biased

Three operating regions of BJT

- Cut off: $V_{CE} = V_{CC}, I_C \cong 0$

- Active or linear : $V_{CE} \cong V_{CC}/2$, $I_C \cong I_{C\,max}/2$

- Saturation: $V_{CE} \cong 0$, $I_C \cong I_{C\,max}$

Q-Point

- The intersection of the dc bias value of I_B with the dc load line determines the *Q*- point.
- It is desirable to have the *Q*-point centered on the load line. Why?
- When a circuit is designed to have a centered *Q*-point, the amplifier is said to be midpoint biased.
- Midpoint biasing allows optimum ac operation of the amplifier.

Introduction - Biasing

The analysis or design of a transistor amplifier requires knowledge of both the dc and ac response of the system.In fact, the amplifier increases the strength of a weak signal by transferring the energy from the applied DC source to the weak input ac signal

- The analysis or design of any electronic amplifier therefore has two components:
- The dc portion and
- The ac portion

During the design stage, the choice of parameters for the required dc levels will affect the ac response.

What is biasing circuit?

- Once the desired dc current and voltage levels have been identified, a network must be constructed that will establish the desired values of I_B, I_C and V_{CE}, Such a network is known as biasing circuit. A biasing network has to preferably make

use of one power supply to bias both the junctions of the transistor.

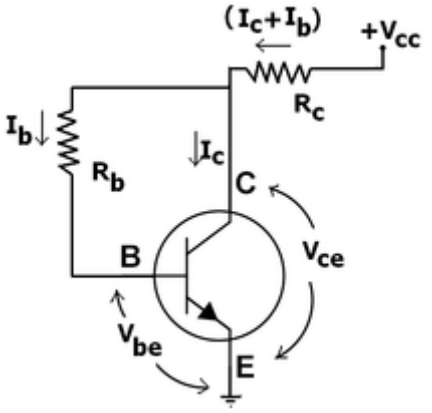
Purpose of the DC biasing circuit

- To turn the device "ON"
- To place it in operation in the region of its characteristic where the device operates most linearly, i.e. to set up the initial dc values of I_B, I_C, and V_{CE}

Important basic relationship

- $V_{BE} = 0.7V$
- $I_E = (\beta + 1)\, I_B \cong I_C$
- $I_C = \beta I_B$

Collector-to-base bias



Collector-to-base bias

This configuration employs negative feedback to prevent thermal runaway and stabilize the operating point. In this form of biasing, the base resistor R_B is connected to the collector instead of connecting it to the DC source V_{CC}. So any thermal runaway will induce a voltage drop across the R_C resistor that will throttle the transistor's base current.

From Kirchhoff's voltage law, the voltage V_{R_b}across the base resistor R_b is

$$V_{R_b} = V_{cc} - \overbrace{(I_c + I_b)R_c}^{\text{Voltage drop across } R_c} - \overbrace{V_{be}}^{\text{Voltage at base}}.$$

By the Ebers–Moll model, $I_c = \beta I_b$, and so

$$V_{R_b} = V_{cc} - (\overbrace{\beta I_b}^{I_c} + I_b)R_c - V_{be} = V_{cc} - I_b(\beta + 1)R_c - V_{be}.$$

From Ohm's law, the base current $I_b = V_{R_b}/R_b$, and so

$$\overbrace{I_b R_b}^{V_{R_b}} = V_{cc} - I_b(\beta + 1)R_c - V_{be}.$$

Hence, the base current I_b is

$$I_b = \frac{V_{cc} - V_{be}}{R_b + (\beta + 1)R_c}$$

If V_{be} is held constant and temperature increases, then the

collector current I_c increases. However, a larger I_c causes the voltage drop across resistor R_c to increase, which in turn reduces the voltage V_{R_b}across the base resistor R_b. A lower base-resistor voltage drop reduces the base current I_b, which results in less collector current I_c. Because an increase in collector current with temperature is opposed, the operating point is kept stable.

Merits:

- Circuit stabilizes the operating point against variations in temperature and β (ie. replacement of transistor)

Demerits:

- In this circuit, to keep I_c independent of β, the following condition must be met:

$$I_c = \beta I_b = \frac{\beta(V_{cc} - V_{be})}{R_b + R_c + \beta R_c} \approx \frac{(V_{cc} - V_{be})}{R_c}$$

which is the case when

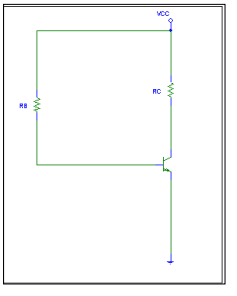
$$\beta R_c \gg R_b.$$

- As β-value is fixed (and generally unknown) for a given transistor, this relation can be satisfied either by keeping R_c fairly large or making R_b very low.
    - If R_c is large, a high V_{cc} is necessary, which increases cost as well as precautions necessary while handling.
    - If R_b is low, the reverse bias of the collector–base region is small, which limits the range of collector voltage swing that leaves the transistor in active mode.
- The resistor R_b causes an AC feedback, reducing the voltage gain of the amplifier. This undesirable effect is a trade-off for greater Q-point stability.

Usage: The feedback also decreases the input impedance of the amplifier as seen from the base, which can be advantageous. Due to the gain reduction from feedback, this biasing form is used only when the trade-off for stability is warranted

Biasing circuits:

- Fixed – bias circuit
- Emitter bias
- Voltage divider bias
- DC bias with voltage feedback
- Miscellaneous bias
- The simplest transistor dc bias configuration.
- For dc analysis, open all the capacitance.



DC Analysis

- Applying KVL to the input loop:

$$V_{CC} = I_B R_B + V_{BE}$$

- From the above equation, deriving for IB, we get,

$$I_B = [V_{CC} - V_{BE}] / R_B$$

- The selection of R_B sets the level of base current for the operating point.
- Applying KVL for the output loop:

$$V_{CC} = I_C R_C + V_{CE}$$

$S(I_{CO}) = \beta + 1$

This indicates poor stability.

Voltage divider configuration

$S(I_{CO}) = (\beta + 1)[1 + R_B / R_E] / [(\beta + 1) + R_B / R_E]$ Here, replace R_B with R_{th}

$S(I_{CO}) = (\beta + 1)[1 + R_{th} / R_E] / [(\beta + 1) + R_{th} / R_E]$

Thus, voltage divider bias configuration is quite stable when the ratio R / R is as small

Physical impact

In a **fixed bias circuit**, I_C increases due to increase in I_{C0}. [$I_C = \beta I_B + (\beta+1) I_{C0}$]

I_B is fixed by V_{CC} and R_B. Thus level of I_C would continue to rise with temperature –

a very unstable situation.

In **emitter bias circuit**, **as I_C increases**, I_E increases, V_E increases. Increase in V_E reduces I_B. $I_B = [V_{CC} - V_{BE} - V_E] / R_B$. A drop in I_B **reduces I_C**.Thus, this configuration is such that there is a reaction to an increase in I_C that will tend to oppose the change in bias conditions.

In the **DC bias with voltage feedback**, as I_C increases, voltage across R_C increases, thus reducing I_B and causing I_C to reduce.

The most stable configuration is **the voltage – divider network**. If the condition βR_E

>>$10R_2$, the voltage V_B will remain fairly constant for changing levels of I_C. V_{BE} =

$V_B - V_E$, as I_C increases, V_E increases, since V_B is constant, V_{BE} drops making I_B to

fall, which will try to offset the increases level of I_C.

S(V_{BE})

$S(V_{BE}) = \Delta I_C / \Delta V_{BE}$

For an emitter bias circuit, $S(V_{BE}) = - \beta / [R_B + (\beta + 1)R_E]$

If $R_E = 0$ in the above equation, we get $S(V_{BE})$ for a fixed bias circuit as, $S(V_{BE}) = - \beta / R_B$.

For an emitter bias,

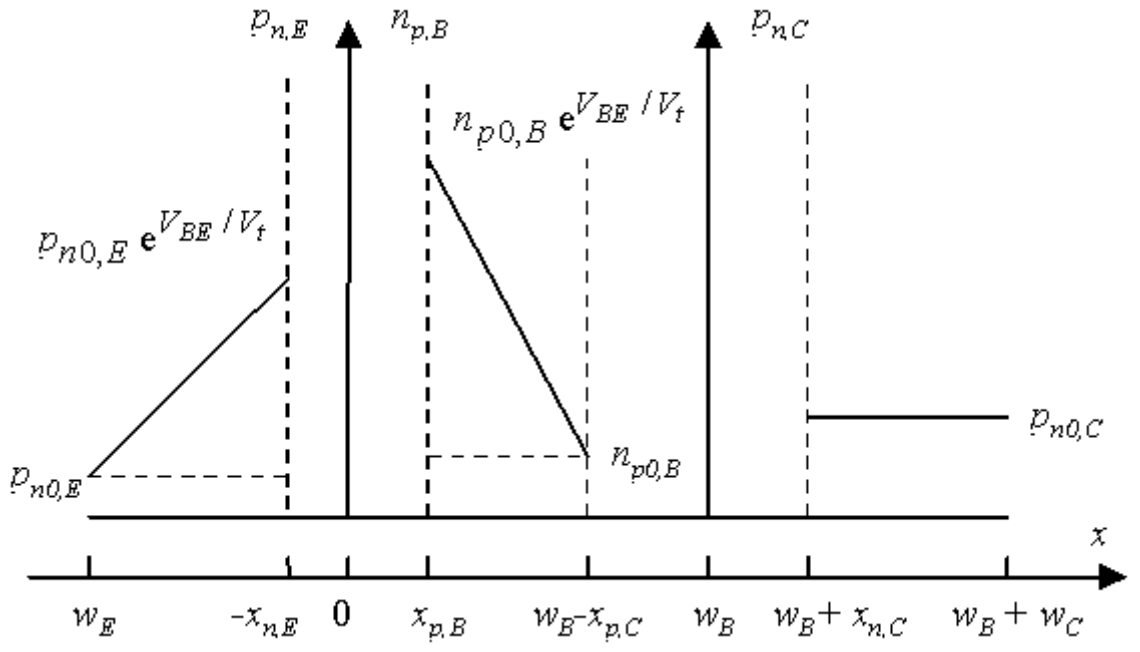
$S(V_{BE}) = - \beta / [R_B + (\beta + 1)R_E]$ can be rewritten as, $S(V_{BE}) = - (\beta/R_E)/ [R_B/R_E + (\beta + 1)]$

If $(\beta + 1) >> R_B/R_E$, then

The larger the R_E, lower the $S(V_{BE})$ and more stable is the system. Total effect of all the three parameters on I_C can be written as,

Forward active mode of operation

The forward active mode is obtained by forward-biasing the base-emitter junction. In addition we eliminate the base-collector junction current by setting $V_{BC} = 0$. The minority-carrier distribution in the quasi-neutral regions of the bipolar transistor, as shown in Figure, is used to analyze this situation in more detail.



Minority-carrier distribution in the quasi-neutral regions of a bipolar transistor (a) Forward active bias mode. (b) Saturation mode.

The values of the minority carrier densities at the edges of the depletion regions are indicated on the Figure. The carrier densities vary linearly between the boundary values as expected when using the assumption that no significant recombination takes place in the quasi-neutral regions. The minority carrier densities on both sides of the base-collector depletion region equal the thermal equilibrium values since V_{BC} was set to zero. While this boundary condition is mathematically equivalent to that of an ideal contact, there is an important difference. The minority carriers arriving at $x = w_B - x_{p,BC}$ do not recombine. Instead, they drift through the base-collector depletion region and end up as majority carriers in the collector region.

$$I_{E,n} = qn_i^2 A_E \left(\frac{D_{n,B}}{N_B w_B'} \right) \left(\exp\left(\frac{V_{BE}}{V_t}\right) - 1 \right)$$

$$I_{E,p} = qn_i^2 A_E \left(\frac{D_{p,E}}{N_E w_E'} \right) \left(\exp\left(\frac{V_{BE}}{V_t}\right) - 1 \right)$$

$$\Delta Q_{n,B} = qA_E \int_{x_{p,E}}^{w_B - x_{p,C}} n_p(x) - n_{p0}\, dx$$

$$\Delta Q_{n,B} = q A_E \frac{n_i^2}{N_B}\left(\exp\left(\frac{V_{BE}}{V_t}\right) - 1\right)\frac{w_B'}{2}$$

And the emitter current due to electrons, $I_{E,n}$, simplifies to:

$$I_{E,n} = \frac{\Delta Q_{n,B}}{t_r}$$

It is convenient to rewrite the emitter current due to electrons, $I_{E,n}$, as a function of the total excess minority charge in the base, $\Delta Q_{n,B}$. This charge is proportional to the triangular area in the quasi-neutral base as shown in Figure and is calculated from

where t_r is the average time the minority carriers spend in the base layer, i.e. the transit time. The emitter current therefore equals the excess minority carrier charge present in the base region, divided by the time this charge spends in the base. This and other similar relations will be used to construct the charge control model of the bipolar junction transistor A combination of equations yields the transit time as a function of the quasi-neutral layer width, w_B', and the electron diffusion constant in the base, $D_{n,B}$.

$$t_r = \frac{w_B'^2}{2D_{n,B}}$$

We now turn our attention to the recombination current in the quasi-neutral base and obtain it from the continuity equation

$$\frac{\partial n_p(x)}{\partial t} = \frac{1}{q}\frac{\partial J_n(x)}{\partial x} - \frac{n_p(x) - n_{p0}}{\tau_n}$$

By applying it to the quasi-neutral base region and assuming steady state conditions:

$$I_{r,B} = qA_E \int_{x_{p,BE}}^{w_B - x_{p,BC}} \frac{n_p(x) - n_{p0}}{\tau_n} dx$$

which in turn can be written as a function of the excess minority carrier charge, $\Delta Q_{n,B}$, using equation

$$I_{r,B} = \frac{\Delta Q_{n,B}}{\tau_n}$$

$$\gamma_E = \frac{1}{1 + \frac{D_{p,E} N_B w_B'}{D_{n,B} N_E w_E'}}$$

It is typically the emitter efficiency, which limits the current gain in transistors made of silicon or germanium. The long minority-carrier lifetime and the long diffusion lengths in those materials justify the exclusion of recombination in the base or the depletion layer. The resulting current gain, under such conditions, is:

$$\beta \cong \frac{D_{n,B} N_E w_E'}{D_{p,E} N_B w_B'}, \quad \text{if} \quad \alpha \cong \gamma_E$$

From this equation, we conclude that the current gain can be larger than one if the emitter doping is much larger than the base doping. A typical current gain for a silicon bipolar transistor is 50 - 150.

$$\alpha_T = 1 - \frac{t_r}{\tau_n} = 1 - \frac{w_B'^2}{2 D_{n,B} \tau_n}$$

This expression is only valid if the base transport factor is very close to one, since it was derived using the "short-diode" carrier distribution. This base transport factor can also be expressed in function of the diffusion length in the base:

$$\alpha_T = 1 - \frac{1}{2}\left(\frac{w_B'}{L_n}\right)^2$$

Uni-junction transistor

The UJT as the name implies, is characterized by a single pn junction. It exhibits negative resistance characteristic that makes it useful in oscillator circuits.

The symbol for UJT is shown in **fig. 1**. The UJT is having three terminals base1 (B1), base2 (B2) and emitter (E). The UJT is made up of an N-type silicon bar which acts as the base as shown in **fig. 2**. It is very lightly doped. A P-type impurity is introduced into the base, producing a single PN junction called emitter. The PN junction exhibits the properties of a conventional diode.

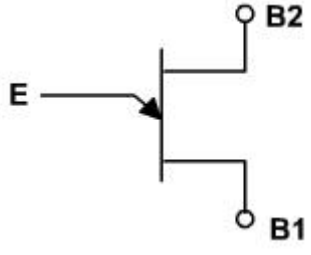


Fig. 1

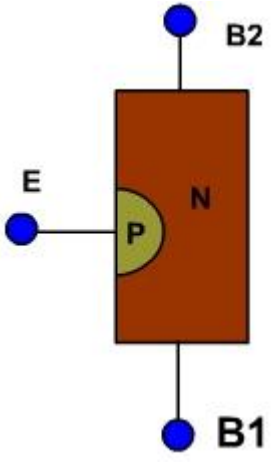


Fig .2

A complementary UJT is formed by a P-type base and N-type emitter. Except for the polarity of voltage and current the characteristic is similar to those of a conventional UJT.

A simplified equivalent circuit for the UJT is shown in **fig. 3**. V_{BB} is a source of biasing voltage connected between B2 and B1. When the emitter is open, the total resistance from B2 to B1 is simply the resistance of the silicon bar, this is known as the inter base resistance R_{BB}. Since the N-channel is lightly doped, therefore R_{BB} is relatively high, typically 5 to 10K ohm. R_{B2} is the resistance between B2 and point ?a', while R_{B1} is the resistance from point ?a' to B1, therefore the interbase resistance R_{BB} is

$R_{BB} = R_{B1} + R_{B2}$

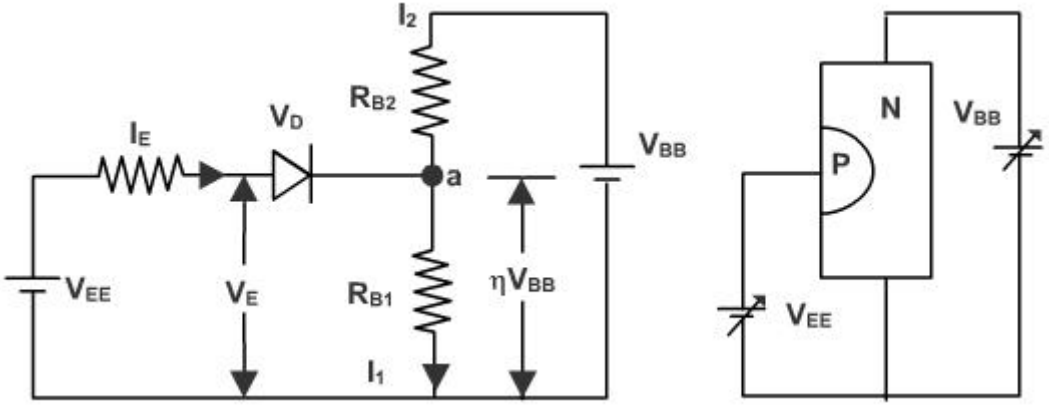


Fig. 3

The diode accounts for the rectifying properties of the PN junction. V_D is the diode's threshold voltage. With the emitter open, $I_E = 0$, and $I_1 = I_2$. The interbase current is given by

$I_1 = I_2 = V_{BB} / R_{BB}$.

Part of V_{BB} is dropped across R_{B2} while the rest of voltage is dropped across R_{B1}. The voltage across R_{B1} is

$V_a = V_{BB} * (R_{B1}) / (R_{B1} + R_{B2})$

The ratio $R_{B1} / (R_{B1} + R_{B2})$ is called intrinsic standoff ratio

$\eta = R_{B1} / (R_{B1} + R_{B2})$ i.e. $V_a = \eta V_{BB}$.

The ratio η is a property of UJT and it is always less than one and usually between 0.4 and 0.85. As long as $I_B = 0$, the circuit of behaves as a voltage divider.

Assume now that v_E is gradually increased from zero using an emitter supply V_{EE} . The diode remains reverse biased till v_E voltage is less than ηV_{BB} and no emitter current flows except leakage current. The emitter diode will be reversed biased.

When $v_E = V_D + \eta V_{BB}$, then appreciable emitter current begins to flow where V_D is the diode's threshold voltage. The value of v_E that causes, the diode to start conducting is called the peak point voltage and the current is called peak point current I_P.

$V_P = V_D + \eta V_{BB}$.

The graph of **fig. 4** shows the relationship between the emitter voltage and current. v_E is plotted on the vertical axis and I_E is plotted on the horizontal axis. The region from $v_E = 0$ to $v_E = V_P$ is called cut off region because no emitter current flows (except for leakage). Once v_E exceeds the peak point voltage, I_E increases, but v_E decreases. up to certain point called valley point (V_V and I_V). This is called negative resistance region. Beyond this, I_E increases with v_E this is the saturation region, which exhibits a positive resistance characteristic.

The physical process responsible for the negative resistance characteristic is called conductivity modulation. When the v_E exceeds V_P voltage, holes from P emitter are injected into N base. Since the P region is heavily doped compared with the N-region, holes are injected to the lower half of the UJT

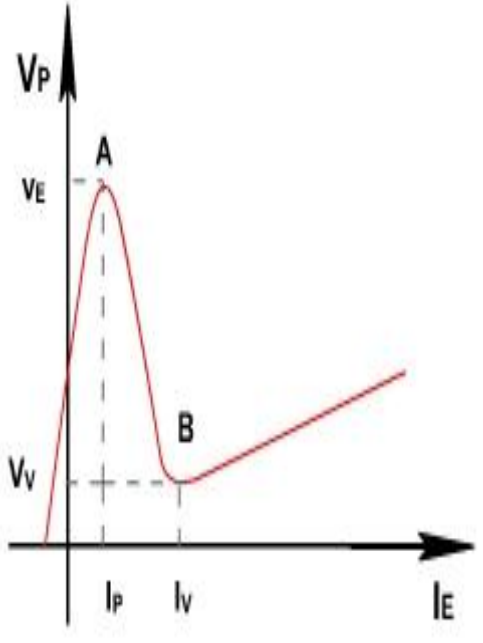


Fig. 4

The lightly doped N region gives these holes a long lifetime. These holes move towards B1 to complete their path by re-entering at the negative terminal of V_{EE}. The large holes create a conducting path between the emitter and the lower base. These increased charge carriers

represent a decrease in resistance R_{B1}, therefore can be considered as variable resistance. It decreases up to 50 ohm.

Since □ is a function of R_{B1} it follows that the reduction of R_{B1} causes a corresponding reduction in intrinsic standoff ratio. Thus as I_E increases, R_{B1} decreases, □ decreases, and V_a decreases. The decrease in V_a causes more emitter current to flow which causes further reduction in R_{B1}, □, and V_a. This process is regenerative and therefore V_a as well as v_E quickly drops while I_E increases. Although R_B decreases in value, but it is always positive resistance. It is only the dynamic resistance between V_V and V_P. At point B, the entire base1 region will saturate with carriers and resistance R_{B1} will not decrease any more. A further increase in I_e will be followed by a voltage rise.

The diode threshold voltage decreases with temperature and R_{BB} resistance increases with temperature because Si has positive temperature coefficient.

UJT Relaxation Oscillator:

The characteristic of UJT was discussed in previous lecture. It is having negative resistance region. The negative dynamic resistance region of UJT can be used to realize an oscillator.

The circuit of UJT relaxation oscillator is shown in **fig. 1**. It includes two resistors R_1 and R_2 for taking two outputs R_2 may be a few hundred ohms and R_1 should be less than 50 ohms. The dc source V_{CC} supplies the necessary bias. The interbase voltage V_{BB} is the difference between V_{CC} and the voltage drops across R_1 and R_2. Usually R_{BB} is much larger than R_1 and R_2 so that V_{BB} approximately equal to V. Note, R_{B1} and R_{B2} are inter-resistance of UJT while R_1 and R_2 is the actual resistor. R_{B1} is in series with R_1 and R_{B2} is in series with R_2 .

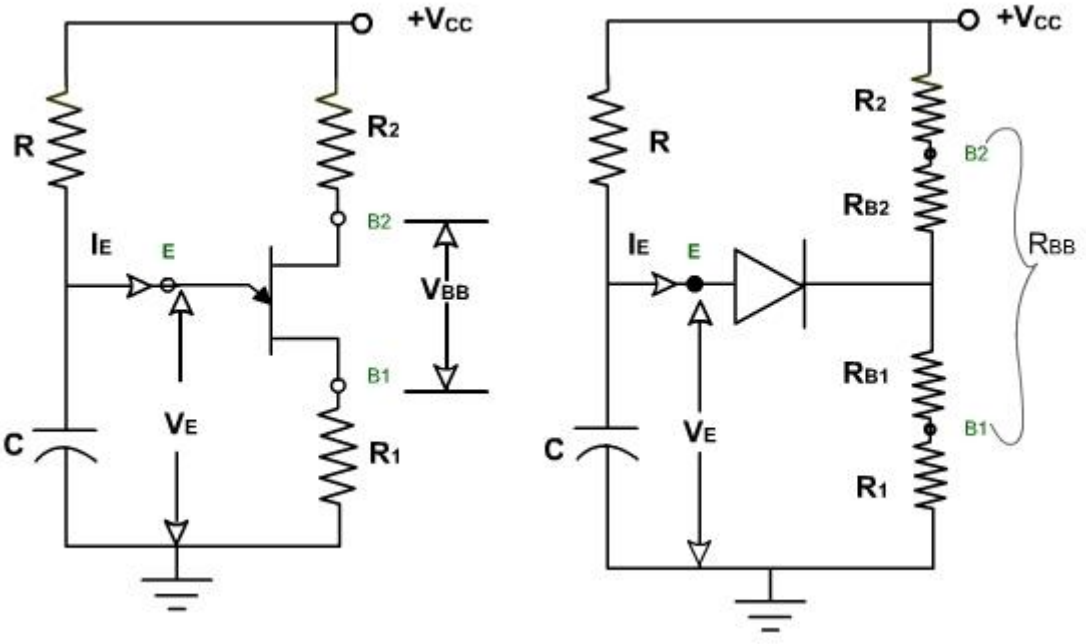


Fig. 1

As soon as power is applied to the circuit capacitor begins to charge toward V. The voltage across C, which is also V_E , rises exponentially with a time constant

□ = R C

As long as $V_E < V_P$, $I_E = 0$. the diode remains reverse biased as long as $V_E < V_P$. When the capacitor charges up to V_P , the diode conducts and R_{B1} decreases and capacitor starts discharging. The reduction in R_{B1} causes capacitor C voltage to drop very quickly to the valley voltage V_V because of the fast time constant due to the low value of R_{B1} and R_1. As soon as V_E drops below $V_a + V_D$ the diode is no longer forward biased and it stops conduction. It now reverts to the previous state and C begins to charge once more toward V_{CC} .

The emitter voltage is shown in **fig. 2**, V_E rises exponentially toward V_{CC} but drops to a very low value after it reaches V_P. The time for the V_E to drop from V_P to V_V is relatively small and usually neglected. The period T can therefore be approximated as follows:

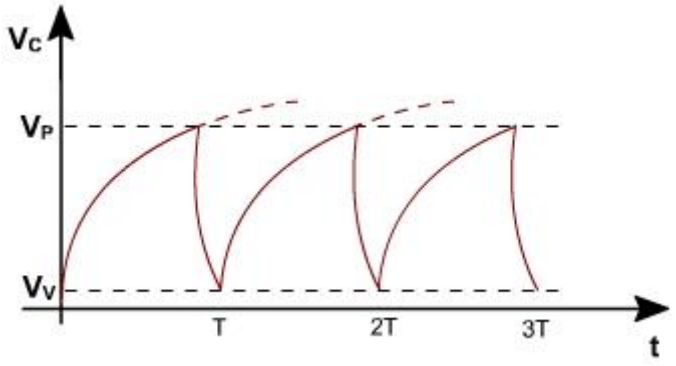


Fig. 2

Let T be the Time required for V_E to rise from 0 to V_P.

As long as $R_{BB} >> (R_1 + R_2)$;

$$V_{BB} \approx V_{CC} \text{ and } V_P = \eta V_{CC}$$

The capacitor charging voltage is given by

$$V_E = V_{CC}\,(1 - e^{-t/RC})$$

Where V_E is the instantaneous capacitor voltage.

Note that at $t = T$, $V_E = V_P = \eta V_{CC}$

$$\eta V = V_{CC}\,(1 - e^{-T/RC})$$

or $$\eta = (1 - e^{-T/RC})$$

or $$e^{-T/RC} = 1 - \eta$$

Thus

$$e^{T/RC} = 1/1 - \eta$$

$$T = RC \ln\left(\frac{1}{1-\eta}\right)$$

$$T = RC\ K$$

The frequency of oscillation is, therefore, given by

$$f_C = \frac{1}{T} \frac{1}{RC\,K}$$

The parameter K varies with η

There are two additional outputs possible for the UJT oscillation one of these is the voltage developed at B1 due to capacitor discharge while the other is voltage developed at B2 as shown in **fig. 3**.

When UJT fires (at t = T) V_a drops, causing a corresponding voltage drop at B2. The duration of outputs at B1 and B2 are determined by C discharge time.

If R_1 is very small, C discharges very quickly and very narrow pulse is produced at the output. If $R_1 = 0$, obviously no pulses appear at B1.

If $R_2 = 0$, no pulse can be generated at B2. If R_1 is too large, its positive resistance may swamp the negative resistance and prevent the UJT form switching back after it has fired.

R_2, in addition to providing a source of pulse at B2, is useful for temperature stabilization of the UJT's peak point voltage .

$V_P = V_D + \square\ V_{BB}$.

As the temperature increases, V_p decreases. The temperature coefficient of R_{BB} is positive. R_s is essentially independent of temperature. It is therefore possible to select R_2 so that $\square\ V_{BB}$ increases with temperature by the same amount as V_D decreases. This provides a constant V_P and, in turn, frequency of oscillation.

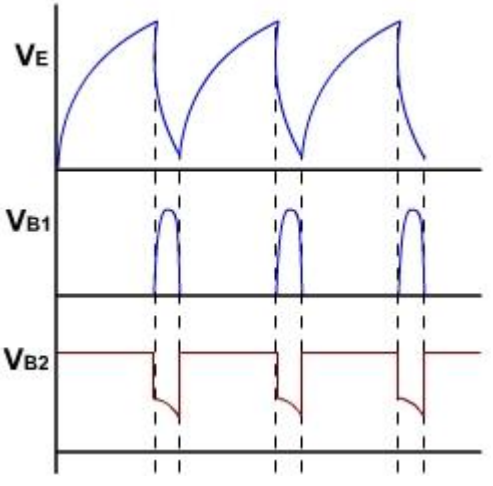


Figure 31.3

Selection of R and C:

In the circuit, R is required to pass only the capacitor charging current. At the instant when V_P is reached; R must supply the peak current. It is therefore, necessary, that the current through R should be slightly greater than the peak point.

$$I_R > I_P$$

$$\frac{V_{CC} - V_P}{R} > I_P$$

$$R < \frac{V_{CC} - V_P}{I_P}$$

Once the UJT fires, V_E drops to the valley voltage V_V . I_E should not be allowed to increases beyond the valley point I_V, otherwise the UJT is taken into saturation region and does not switch back, R therefore must be selected large enough to ensure that

$$I_E < I_V$$

$$\frac{V_{CC} - V_V}{R} < I_V$$

$$R > \frac{V_{CC} - V_V}{I_V}$$

$$\text{Therefore, } \frac{V_{CC} - V_V}{I_P} > R > \frac{V_{CC} - V_V}{I_V}$$

As long as R is chosen between these extremes, reliable operation results.