MODULE – 5

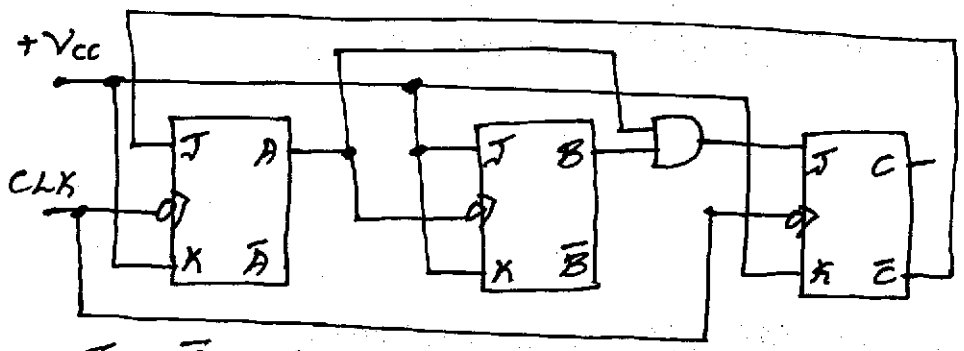
COUNTERS & D/A CONVERSION AND A/D CONVERSION

COUNTERS

DECADE COUNTERS:

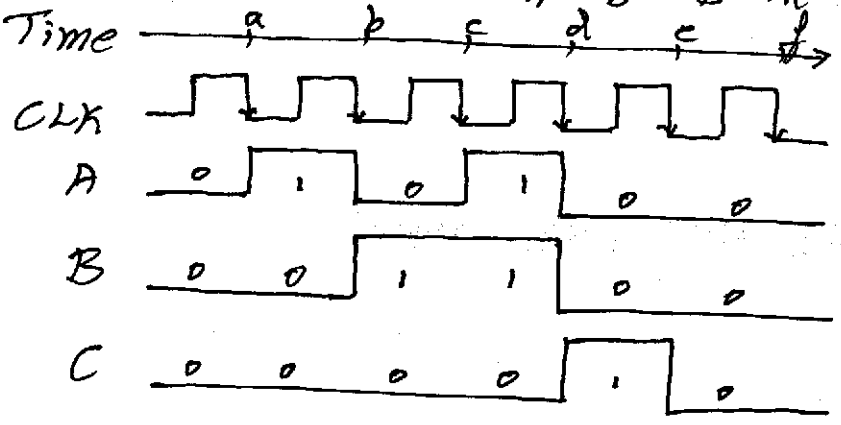
A Mod-5 Counter:

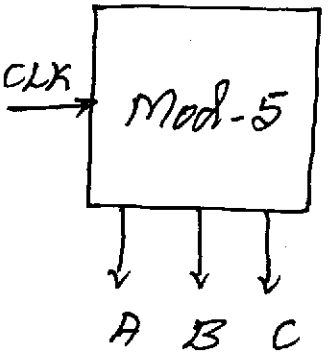
A three flip-flop counter has a natural count of 8. The following counter is constructed such that, it will skip over three counts, and gives a mod-5 counter.



C	B	A	Count
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
0	0	0	0 repeats

$J_A = \bar{C}$, $J_C = AB$, $K_A = J_B = K_B = K_C = 1$.

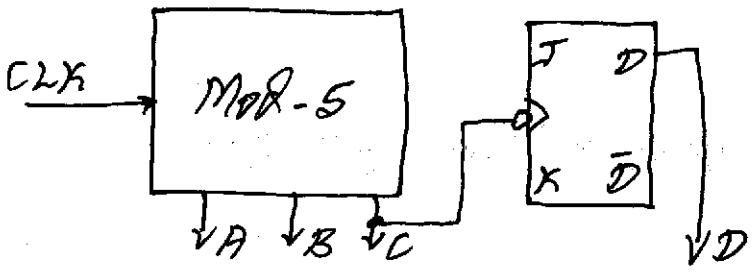




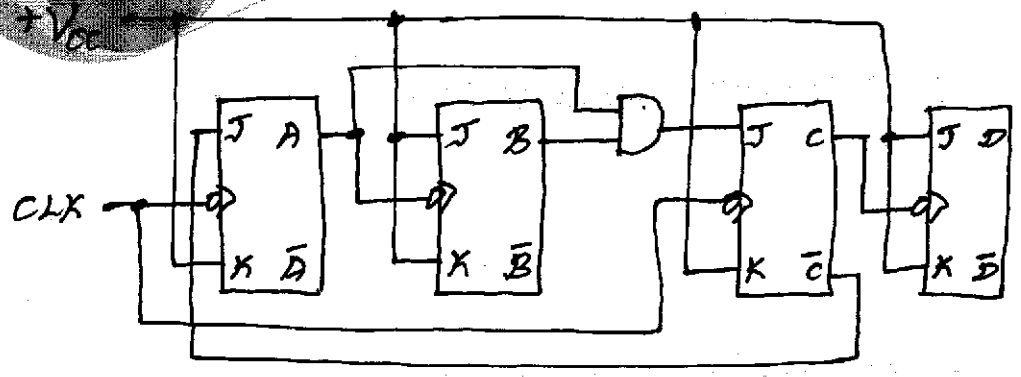
Mod-5 Binary Counter

A Mod-10 Counter (5 x 2, Mod-10 Counter):

A 5 x 2, mod-10 counter is shown in the following Fig.

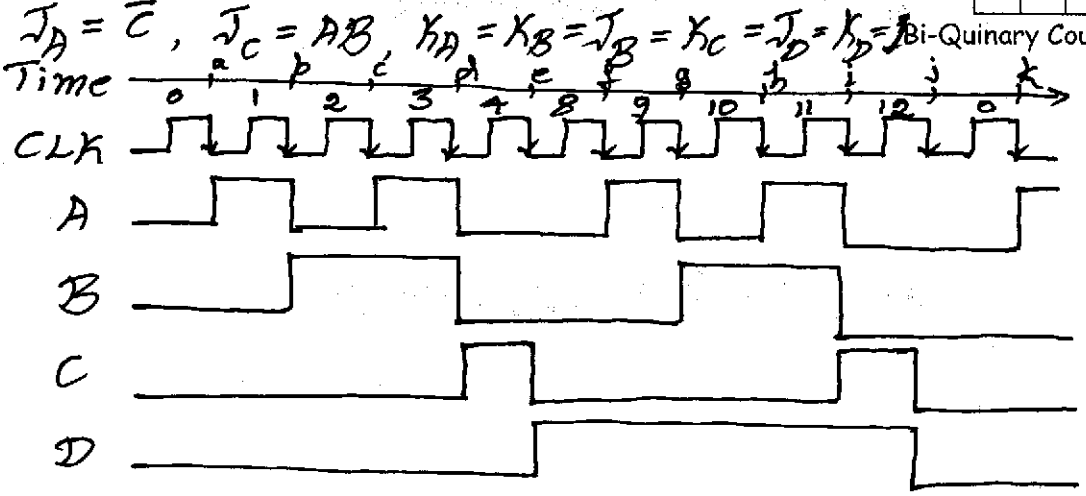


D	C	B	A	Count
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3



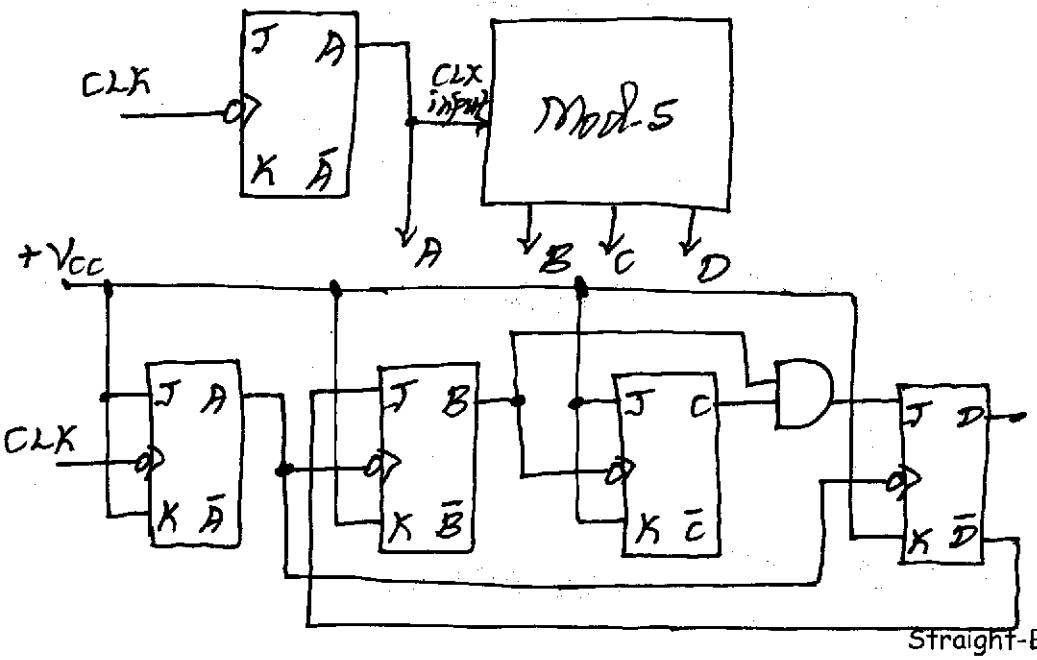
0	1	0	0	4
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
0	0	0	0	0 repeats

Bi-Quinary Count Sequence



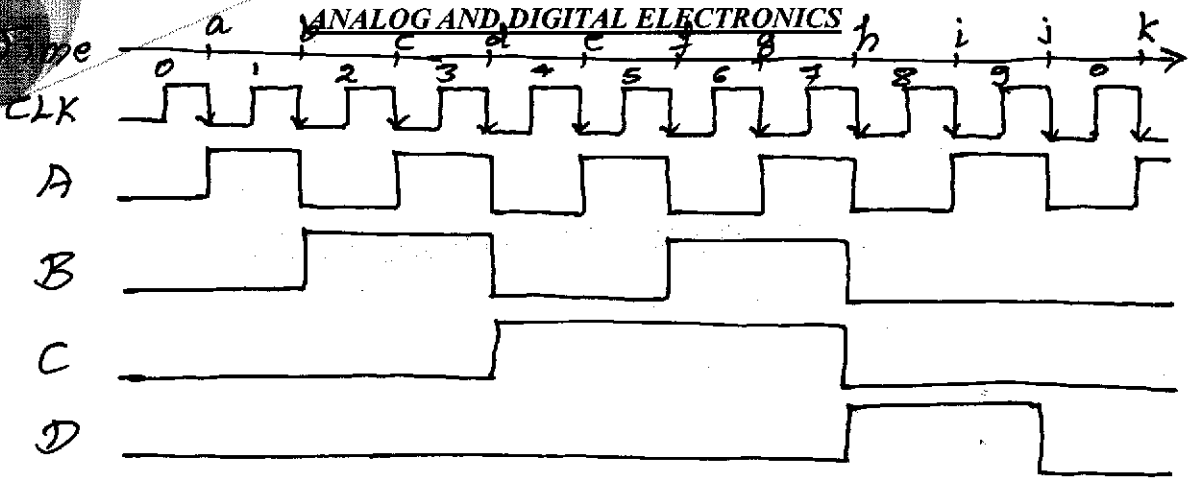
A Mod-6 Counter (2 x 3, Mod-6 Counter):

A 2 x 3, mod-6 counter is shown in the following Fig.

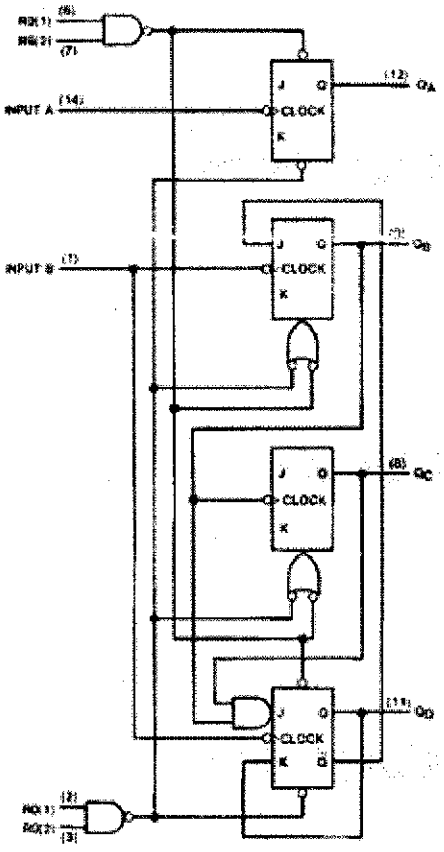


D	C	B	A	Count
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
0	0	0	0	0 repeats

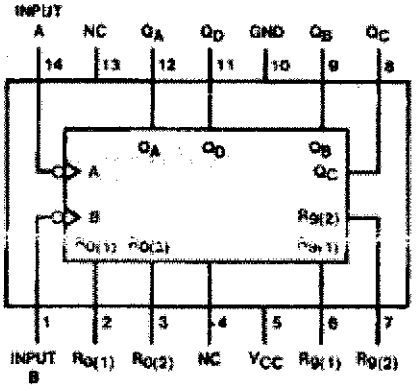
Straight-Binary Count Sequence



The 7490A: The 54/7490A is a TTL MSI decade counter. Its logic diagram, pin-out, and truth table are given in the following Fig.



Dual-In-Line Package



Reset/Count Function Table

Reset Inputs				Outputs			
R0(1)	R0(2)	R9(1)	R9(2)	Q_D	Q_C	Q_B	Q_A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

Note 1: H = High Level, L = Low Level, X = Don't Care.

Note 2: Output Q_A is connected to input B for BCD count.

Note 3: Output Q_D is connected to input A for bi-quinary count.

Count	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
Output Q_A connected to input B				

Count	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
8	H	L	L	6
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
Output Q_D connected to input A				

PRESETTABLE COUNTERS:

Self Study.

COUNTER DESIGN AS A SYNTHESIS PROBLEM:

Here, we consider counter as a state machine and discuss counter design steps:

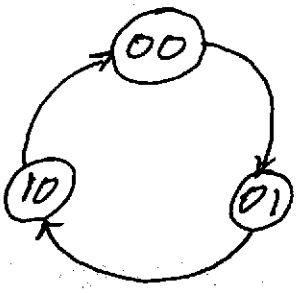
1. Draw the *state diagram* for the problem
2. Construct the *truth table*
3. Construct the *transition table*
4. Write *excitation table* (by using characteristic table and state diagram of flip-flop) for flip-flop used in design
5. Construct *state table* by using transition table and excitation table
6. Draw the *K-map* and solve for *logic equation*; and finally, draw the *logic diagram.*

Problem: *Design a mod-3 counter as a synthesis problem using JK flip-flop.*

Solution:

A mod-3 counter will generate 0, 1 , 2, 0, . . . states.

1. State Diagram:



2. Truth Table:

Clock Count	B	A
0	0	0
1	0	1
2	1	0
3	0	0

Transition Table:

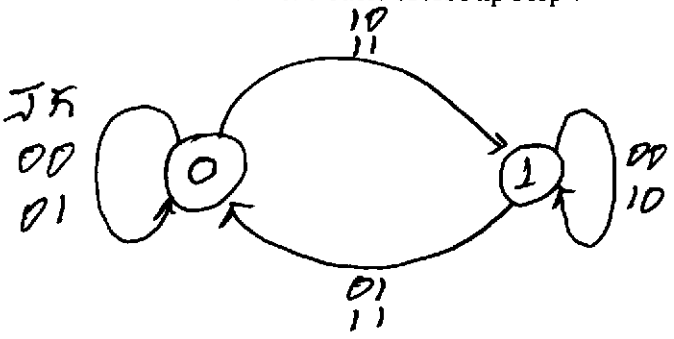
Present State		Next State	
B	A	B	A
0	0	0	1
0	1	1	0
1	0	0	0

J	K	Q_{n+1}	Action
0	0	Q_n	No Change
0	1	0	RESET
1	0	1	SET
1	1	$\overline{Q_n}$	Toggle

/*Characteristic Table of JK Flip-Flop*/

4. Excitation Table for JK Flip-Flop:

Flip-Flop Output		Flip-Flop Input	
Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

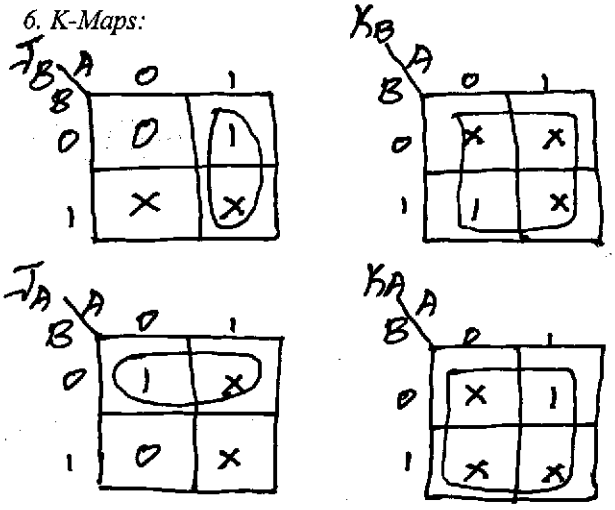


/*Sate Diagram for KJ Flip-Flop*/

5. State Table:

Present State		Next State		Flip-Flop Inputs			
B	A	B	A	J_B	K_B	J_A	K_A
0	0	0	1	0	X	1	X
0	1	1	0	1	X	X	1
1	0	0	0	X	1	0	X
1	1	X	X	X	X	X	X

6. K-Maps:



$J_B = A$ $\quad K_B = 1$

$J_A = \bar{B}$ $\quad K_A = 1$

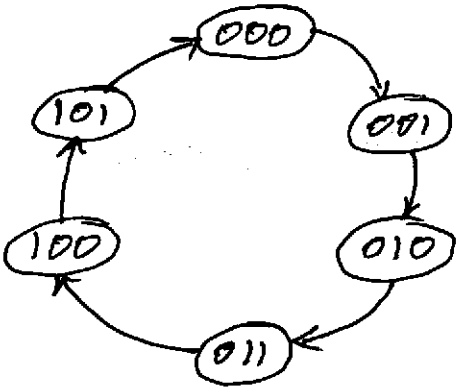
Logic Diagram:

Problem: *Design a mod-6 counter as a synthesis problem using JK flip-flop.*

Solution:

A mod-6 counter will generate 0, 1 , 2, 3, 4,5, . . . states.

State Diagram:



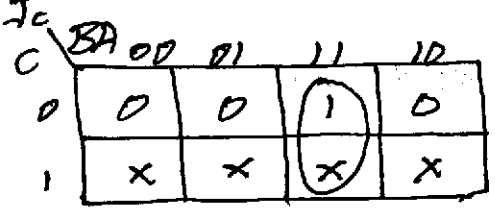
Truth Table:

Clock Count	C	B	a
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1

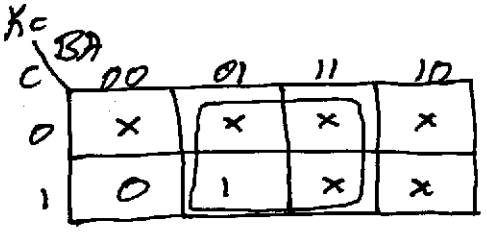
Sate Table:

Present State			Next State			Flip-Flop Inputs					
C	B	A	C	B	A	J_C	K_C	J_B	K_B	J_A	K_A
0	0	0	0	0	1	0	x	0	x	1	x
0	0	1	0	1	0	0	x	1	x	x	1
0	1	0	0	1	1	0	x	x	0	1	x
0	1	1	1	0	0	1	x	x	1	x	1
1	0	0	1	0	1	x	0	0	x	1	x
1	0	1	0	0	0	x	1	0	x	x	1
1	1	0	X	X	X	X	X	X	X	X	X
1	1	1	X	X	X	X	X	X	X	X	X

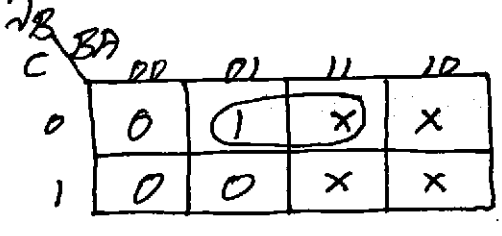
K-Maps:



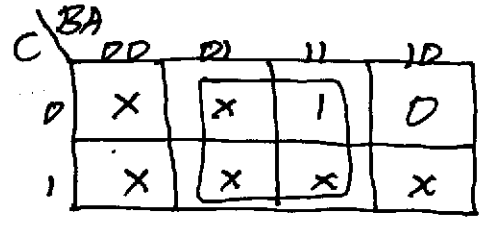
$J_C = BA$



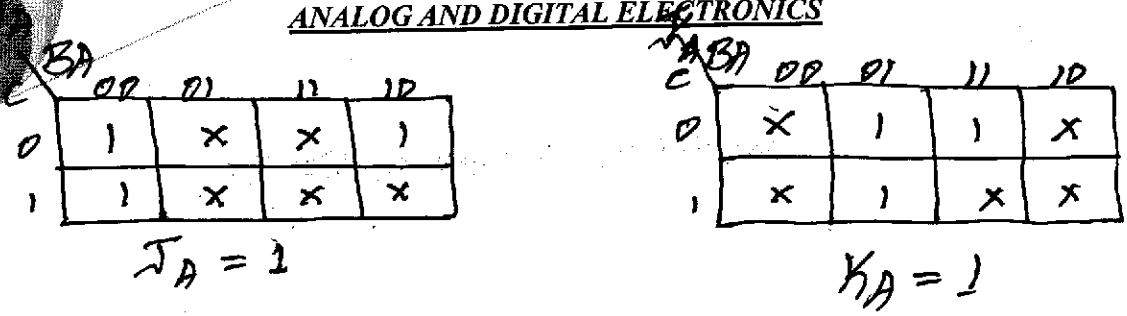
$K_C = A$



$J_B = A\bar{C}$



$K_B = A$



Logic Diagram:

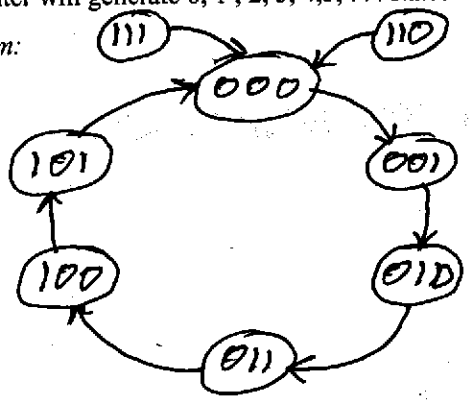
NOTE: In the above problem, for the design, initially, when the power is switched on, if circuit enters to an invalid state (state 6 or state 7), then *lock-in condition* results. The designed counter will not give proper result. The solution is self *correcting mod-6 counter*.

Problem: *Design a self correcting mod-6 counter as a synthesis problem using JK flip-flop.*

Solution:

A mod-6 counter will generate 0, 1 , 2, 3, 4,5, . . . states.

State Diagram:



Truth Table:

Clock Count	C	B	a
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1

Sate Table:

Present State	Next State	Flip-Flop Inputs

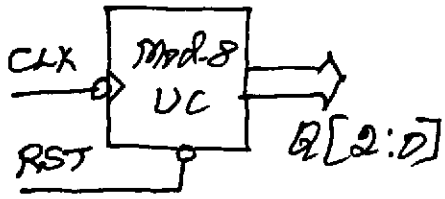
C	B	A	C	B	A	J_C	K_C	J_B	K_B	J_A	K_A
0	0	0	0	0	1	0	x	0	x	1	x
0	0	1	0	1	0	0	x	1	x	x	1
0	1	0	0	1	1	0	x	x	0	1	x
0	1	1	1	0	0	1	x	x	1	x	1
1	0	0	1	0	1	x	0	0	x	1	x
1	0	1	0	0	0	x	1	0	x	x	1
1	1	0	0	0	0	x	1	x	1	0	x
1	1	1	0	0	0	x	1	x	1	x	1

K-Maps: $J_C = BA$ $K_C = B + A$ $J_B = A\bar{C}$ $K_B = A + C$ $J_A = \bar{C} + \bar{B}$ $K_A =$

Logic Diagram:

DIGITAL CLOCK:

Self Study.



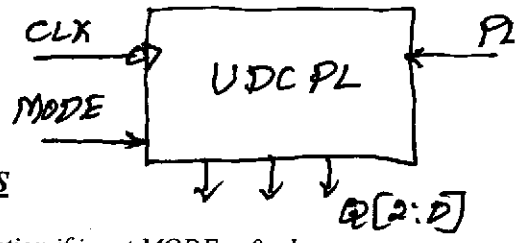
COUNTER DESIGN USING HDL:

Mod-8 Up Counter:

```
module UC (CLK, RST, Q);
input CLR, RST;
output [2:0] Q; reg [2:0] Q;
always @ (negedge CLR or negedge RST)
  if (~RST) Q = 3'b0;
  else Q = Q + 1;
endmodule
```

If a particular type of flip-flop to be used for the counter; the Verilog code will be as follows:

```
module UCJK (A, B, CLK, RST);
output A, B; // Module-3 requires 2 FFs.
wire JA, JB, KA, KB;
assign JA = ~B;     assign KA = 1'b1;
assign JB = A;      assign KB = 1'b1;
JKFF JK1 (A, JA, KA, CLK, RST); // instantiating JKFF
JKFF JK2 (B, JB, KB, CLK, RST); // ---" ---
endmodule
module JKFF (Q, J, K, CLK, RST);
input CLR, RST, J, K; output Q; reg Q;
always @ (negedge CLR or negedge RST)
  if (~RST) Q = 1'b0;
  else Q <= (J & ~Q) | (~K & Q);
endmodule
```



Problem: *Design a modulo-8 up down counter which counts in upward direction if input MODE = 0, else counts in downward direction. It should also have a parallel load facility; when PL = 1, a 3-bit number D is asynchronously loaded to the counter. The counter counts at the negative-edge of CLOCK and its output is represented by Q.*

Solution: The Verilog HDL code for the problem is given below. We have used a new keyword ***integer*** to hold a value temporarily. This helps us in writing both up and down count in one single statement that responds to CLOCK within ***always*** block.

```
module UDCPL (CLR, PL, MODE, D, Q); // Up Down counter
input CLR, PL, MODE;                // with parallel load.
input [2:0] D;
output [2:0] Q; reg [2:0] Q; // Mod-8 reg. 3 FFs.
integer updown; // updown will be +1 or -1 depending on MODE
always @(negedge CLR)
  begin
    if (MODE) updown = -1; // If MODE=1, counts up.
    else updown = 1;
    if (PL) Q = D; // If PL=1, parallel loading takes place
    else Q = Q + updown; // Responds to CLK.
  end
endmodule
```

D/A CONVERSION AND A/D CONVERSION

VARIABLE, RESISTOR NETWORKS:

Converting a digital signal into an equivalent analog signal is accomplished by designing a resistive network that will change each digital digit level into an equivalent binary weighted voltage (or current).

Binary Equivalent Weight:

Consider the truth table of a 3-bit binary signal. Suppose that, we want to change the eight possible digital signals of this truth table into equivalent analog voltages.

The smallest number represented is 000; let us make this equal to 0 V. The largest number is 111; let us make this equal to +7 V. This establishes the range of analog signal to be developed.

Between 000 and 111, there are seven discrete levels. Therefore, divide the analog signal into seven levels.

2^2	2^1	2^0
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

The smallest incremental change in the digital signal is represented by (the LSB), 2^0. Hence, a 1 in 2^0 position will cause a change of +7 * (1/7) = +1 V, at the output. Similarly, a 1 in 2^1 position will cause a change of +7 * (2/7) = +2 V, at the output; and a 1 in 2^2 position will cause a change of +7 * (4/7) = +4 V, at the output.

The process can be continued; and it is seen that each successive bit will have a value twice that of the preceding bit. The binary equivalent weight of LSB is 1/7, next LSB is 2/7 and MSB (in a 3-bit system) is 4/7. The sum of the weights must be equal to 1 (1/7 + 2/7 + 4/7 = 1). Hence, in general; $LSB\ weight = \frac{1}{(2^n - 1)}$

The remaining weights are found by multiplying by 2, 4, 8, and so on.

Problem: *Find the binary equivalent weight of each bit in a 3- bit system and 4-bit system.*

Solution:

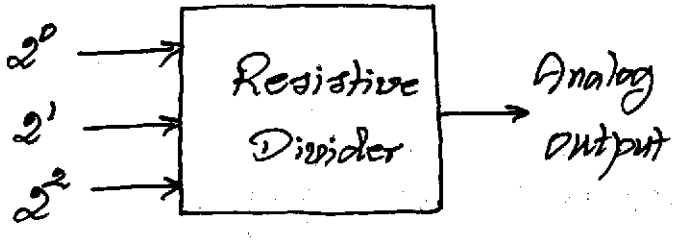
Bit	Weight
2^0	1/7
2^1	2/7
2^2	4/7
Sum	7/7

Bit	Weight
2^0	1/15
2^1	2/15
2^2	4/15
2^3	8/15
Sum	15/15

In a 3-bit system, the LSB has a weight of $1/(2^3 - 1) = 1/7$. The second LSB has a weight of 2 * 1/7 = 2/7. The MSB has a weight of 4 * 1/7 = 4/7. Thus, the sum is 1/7 + 2/7 + 4/7 = 7/7 = 1.

In a 4-bit system, the LSB has a weight of $1/(2^4 - 1) = 1/15$. The second LSB has a weight of 2 * 1/15 = 2/15. The third LSB has a weight of 4 * 1/15 = 4/15. The MSB has a weight of 8 * 1/15 = 8/15. Thus, the sum is 1/15 + 2/15 + 4/15 + 8/15 = 15/15 = 1.

Resistive Divider: A resistive divider has three digital inputs and one analog out, as shown in the following Fig. Assume that, the digital input levels are 0 = 0V and 1 = +7 V. Based on this analog range; the output analog voltage for all the discrete digital inputs are listed below.

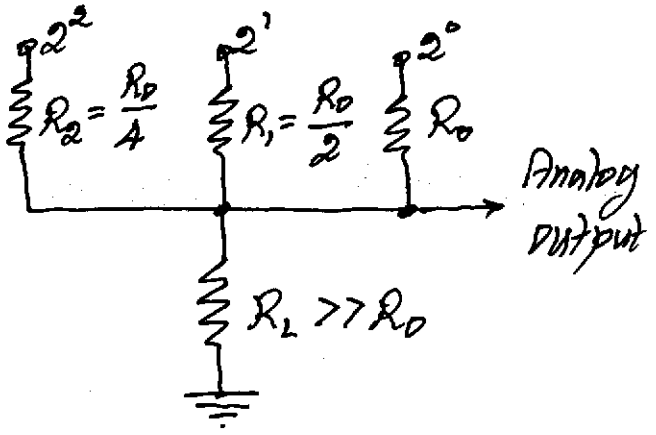


Digital Inputs			Analog Output
0	0	0	+0 V
0	0	1	+1 V
0	1	0	+2 V
0	1	1	+3 V
1	0	0	+4 V
1	0	1	+5 V
1	1	0	+6 V
1	1	1	+7 V

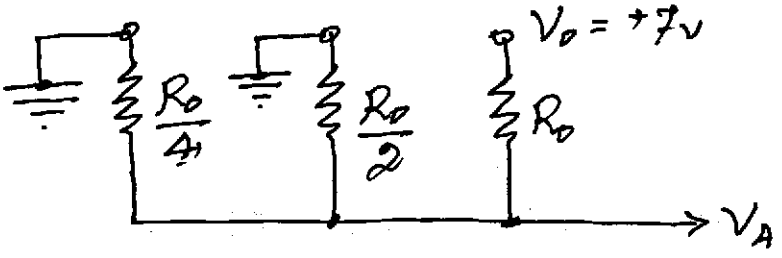
The resistive divider must do two things in order to change the digital input into an equivalent analog output voltages:

1. The 2^0 bit must be changed to +1 VC, and the 2^1 bit must be changed to +2 V, and the 2^2 bit must be changed to +4 V.
2. These three voltages representing the digital bits must be summed together to form the analog output voltage.

A resistive divider that performs these three functions is shown in the following Fig. Resistor R_0, R_1, and R_2 from the divider network. Resistance R_L represents the load.



Assume that the digital input signal is 001 is applied to this network. For the digital input 001, the equivalent resistive divider circuit is drawn below.



The analog output voltage, V_A, can be found by *Millman's theorem – the voltage appearing at any node in a resistive network is equal to the summation of the currents entering the node divided by the summation of the conductances connected to the node*; i.e. $V = \frac{\frac{V_1}{R_1}+\frac{V_2}{R_2}+\frac{V_3}{R_3}+\ldots}{\frac{1}{R_1}+\frac{1}{R_2}+\frac{1}{R_3}+\ldots}$

Applying Millman's theorem to the above network, we obtain;

$$V_A = \frac{\frac{V_0}{R_0}+\frac{V_1}{R_0/2}+\frac{V_2}{R_0/4}}{\frac{1}{R_0}+\frac{1}{R_0/2}+\frac{1}{R_0/4}} = \frac{7/R_0}{\frac{1}{R_0}+\frac{2}{R_0}+\frac{4}{R_0}} = \frac{7}{7} = +1\,V$$

Thus, the output V_A can be found for any digital input signal by using the following modified form of Millman's theorem: $V_A = \frac{V_0 2^0 + V_1 2^1 + V_2 2^2 + V_3 2^3 + \ldots + V_{n-1} 2^{n-1}}{(2^n - 1)}$

where, V_0, V_1, V_2, V_3, . . . , V_{n-1} are the digital input voltage levels (0 or V) and the n is the number of input bits.

Problem: *For a 5-bit resistive divider, determine the following: (a) the weight assigned to the LSB; (b) the weight assigned to the 2nd and 3rd LSB; (c) the change in output voltage due to a change in the LSB, the 2nd LSB, and the 3rd LSB; (d) the output voltage for a digital input of 10101. Assume 0 = 0 V and 1 = +10 V.*

Solution:

(a) For a 5-bit resistive divider, the LSB weight is: $1/(2^5 - 1) = 1/31$.

(b) The 2nd LSB weight is: $2 * 1/(2^5 - 1) = 2/31$. The 3rd LSB weight is: $4 * 1/(2^5 - 1) = 4/31$.

(c) The LSB causes a change in the output voltage of 10/31 V. The 2nd LSB causes a change in the output voltage of 20/31 V. The 3rd LSB causes a change in the output voltage of 40/31 V.

(d) The output voltage for the digital input of 10101 is: $V_A = \frac{10*2^0 + 0*2^1 + 10*2^2 + 0*2^3 + 10*2^4}{(2^5 - 1)}$

$= [10\,(1 + 4 + 16)]/31 = 210/31 = +6.77\text{V}$

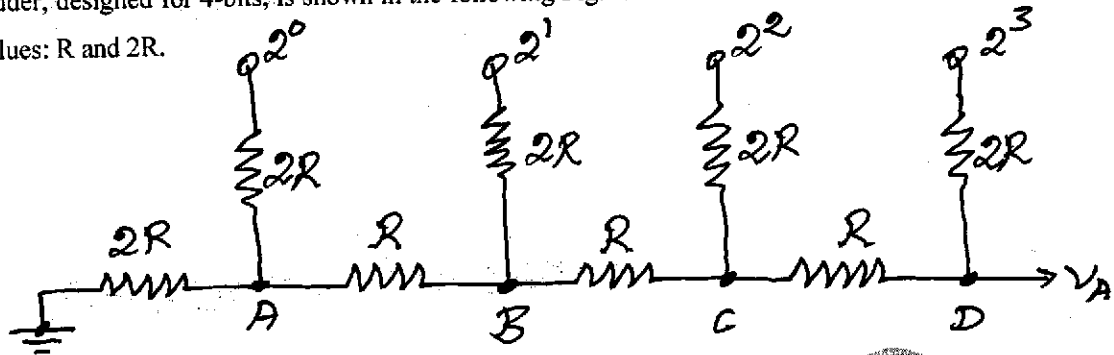
Drawbacks:

1. Each resistor in the network has a different value. Since these dividers are usually constructed by using precision resistors, the added expense becomes unattractive.
2. The resistor used for the MSB is required to handle a much greater current that that used for LSB resistor. For example, in 10-bit system, the current through MSB resistor is approximately 500 times as large as the current through the LSB resistor.

For these reasons, another type of resistive network, called a *ladder*, has been developed.

BINARY LADDER:

A *binary ladder* is a resistive network, whose output voltage is a properly weighted sum of the digital inputs. Such a ladder, designed for 4-bits, is shown in the following Fig. It is constructed of resistors that have only two values: R and 2R.



Let us now examine the resistive properties of the network, assuming that all the digital inputs are at ground. Beginning at node A, the total resistance looking into the terminating resistor is 2R. The total resistance looking out towards 2^0 input is also 2R. These two resistors can be combined to form an equivalent resistor of value R as shown in Fig (a) below.

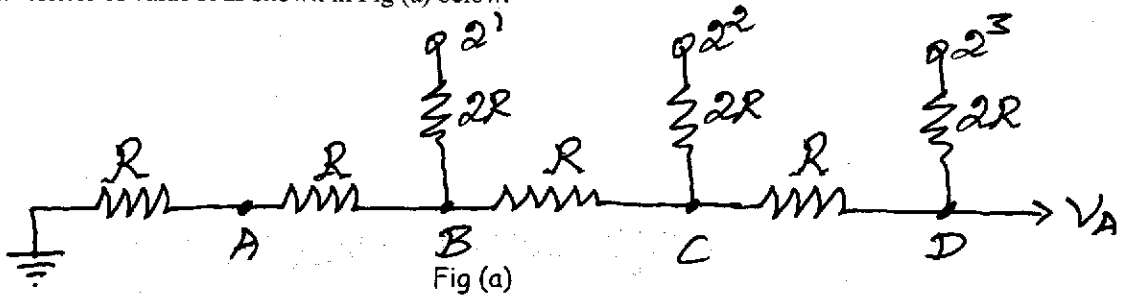


Fig (a)

Now, moving to node B, we see that the total resistance looking into the branch toward node A is 2R, as is the total resistance looking out toward the 2^1 input. These resistors can be combined to simplify the network, as shown in Fig (b) below.

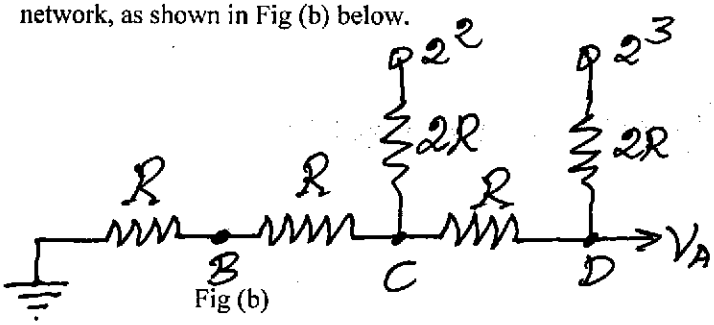


Fig (b)

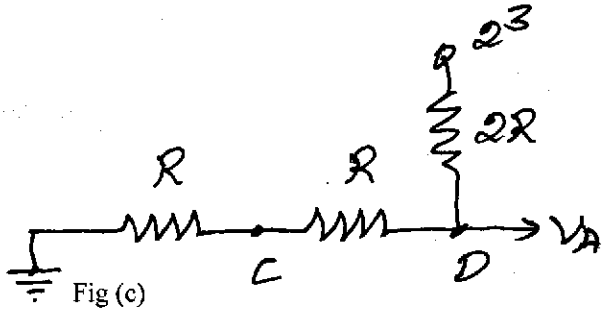


Fig (c)

In the similar fashion, in the network shown in Fig (b); the resistance looking back toward node C is 2R, as is the resistance looking out toward the 2^2 input. Hence, network in Fig (b) can be simplified as network shown in Fig (c).

From this equivalent circuit (Fig (c)); it is clear that, the resistance looking back toward node C is 2R, as is the resistance looking out toward the 2^3 input.

We can conclude that, the total resistance looking from any node back toward the terminating resistor or out toward the digital input is 2R.

Now, assume that, the digital input is 1000. With this input signal, the binary ladder can be drawn as shown in Fig (d) below. Since there are no voltage sources to the left of node D, the entire network to the left of node D can be replaced by a resistance of 2R to form the equivalent circuit shown in Fig (e) below.

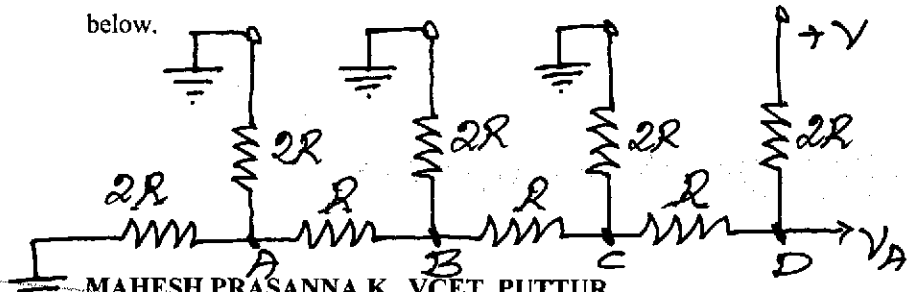


Fig (d)

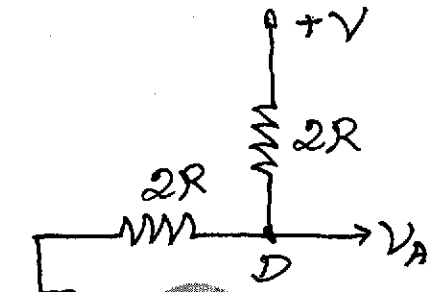


Fig (e)

From this equivalent circuit, it can be easily seen that the output voltage is: $V_A = V * \frac{2R}{2R+2R} = \frac{+V}{2}$

Thus, a 1 in MSB position will provide an output voltage of +V/2.

Similarly, it can be shown that, a 1 in second MSB position will provide an output voltage of +V/4; a 1 in third MSB position will provide an output voltage of +V/8; and a 1 in LSB position will provide an output voltage of +V/16.

Problem: *What are the output voltages caused by each bit in a 5-bit ladder, if the input levels are 0 = 0 V and 1 = +10 V?*

Solution: The output voltages caused by each bit in a 5-bit ladder are given below:

First MSB $V_A = \frac{+V}{2} = \frac{+10}{2} = +5\ V$

Second MSB $V_A = \frac{+V}{4} = \frac{+10}{4} = +2.5\ V$

Third MSB $V_A = \frac{+V}{8} = \frac{+10}{8} = +1.25\ V$

Fourth MSB $V_A = \frac{+V}{16} = \frac{+10}{16} = +0.625\ V$

LSB = Fifth MSB $V_A = \frac{+V}{32} = \frac{+10}{32} = +0.3125\ V$

NOTE:

Bit Position	Binary Weight	Output Voltage
MSB	1/2	V/2
2nd MSB	1/4	V/4
3rd MSB	1/8	V/8
4th MSB	1/16	V/16
5th MSB	1/32	V/32
.	.	.
.	.	.
.	.	.
Nth MSB	$1/2^N$	$V/2^N$

Based on the principle of Superposition;

the total output voltage due to the combination of input digital levels, can be found by simply taking the sum of the output levels caused by each digital input individually.

In equation form, the output voltage is given by; $V_A = \frac{V}{2} + \frac{V}{4} + \frac{V}{8} + \frac{V}{16} + \ ... + \frac{V}{2^n}$

where *n* is the total number of bits at the input.

This equation can be simplified as; $V_A = \frac{V_0 2^0 + V_1 2^1 + V_2 2^2 + V_3 2^3 + ... + V_{n-1} 2^{n-1}}{2^n}$

where $V_0, V_1, V_2, \ldots, V_{n-1}$ are the digital input voltage levels.

Problem: *Find the output voltage from a 5-bit ladder that has a digital input of 11010. Assume that 0 = 0 V and 1 = +10 V.*

Solution: The output of a 5-bit ladder for the digital input 11010 is given by;

$$V_A = \frac{0*2^0 + 10*2^1 + 0*2^2 + 10*2^3 + 10*2^4}{2^5} = \frac{[10(2+8+16)]}{32} = \frac{10*26}{32} = +8.125\ V$$

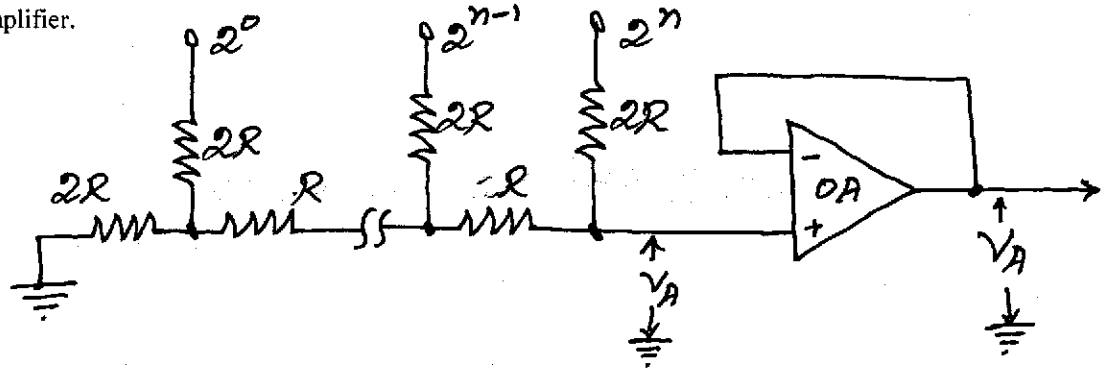
NOTE: The full-scale voltage for the ladder is given by; $V_A = V(\frac{1}{2} + \frac{1}{4} + \frac{1}{8} + \frac{1}{16} + \ldots + \frac{1}{2^n})$

Problem: *What is the full-scale output voltage of the 5-bit ladder which has a digital input of 11010?*

Solution: The full-scale voltage is simply the sum of the individual bit voltages; thus

$$V = 5 + 2.5 + 1.25 + 0.3125 = +9.6875\ V$$

The Operational Amplifier (OA) can be connected to the binary ladder as a unity-gain non-inverting amplifier.



Connecting an OA to Binary Ladder

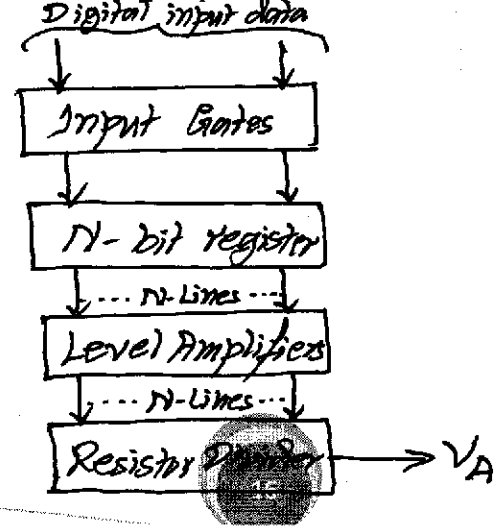
D/A CONVERTERS:

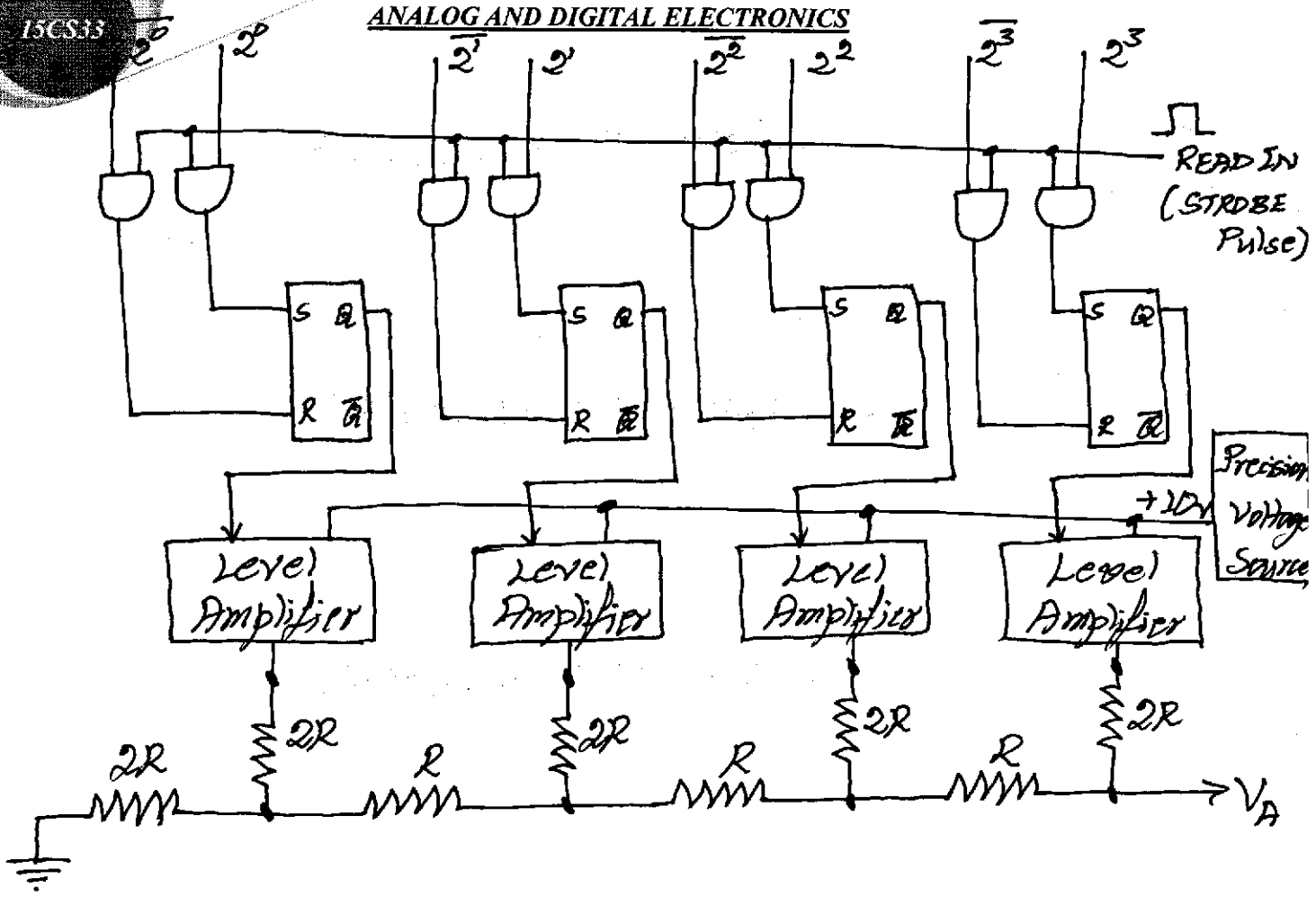
The resistive divider or the ladder can be used as the basis for a digital-to-analog (D/A) converter. The resistive network translates digital signal to an analog voltage. Additional circuitry is required to complete the design of the D/A converter.

- There must be a *register* that can be used to store the digital information. This register could be any one of the many types discusses.
- There must also be level *amplifiers* between the register and the resistive network to ensure that the digital signals presented to the network are all of the same level and constant.
- There must be some form of *gating* on the input of the register such that the flip-flops can be set with the proper information from the digital system.

A complete digital-to-analog converter in block diagram form is shown.

A complete schematic for 4-bit D/A converter is shown in the following Fig.





4-Bit D/A Converter

Each level amplifier have two inputs: one input is the +10 V from the precision voltage source, and the other is from a flip-flop. The amplifiers work in such a way that, when the input from a flip-flop is high, the output of the amplifier is +10 V; and when the input from the flip-flop is low, the output is 0 V.

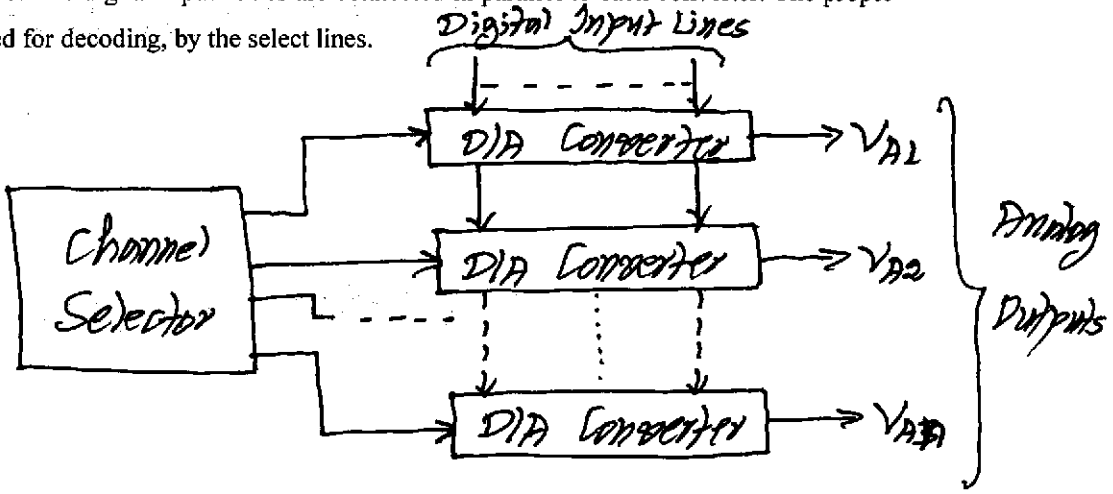
Out of four flip-flops, the flip-flop on the right represents the MSB, and the flip-flop on the left represents the LSB. Each flip-flop requires a positive level at the R or S input to reset or set it.

The gating scheme for entering information into the register is straightforward. When the READ IN line goes high, only one of the two gate outputs connected to each flip-flop is high, and the flip-flop is set or reset accordingly. Thus, data are entered into the register, each time the READ IN pulse occurs.

Multiple Signals: Quite often, it is necessary to decode more than one signal. We have two ways in which the signals can be decoded.

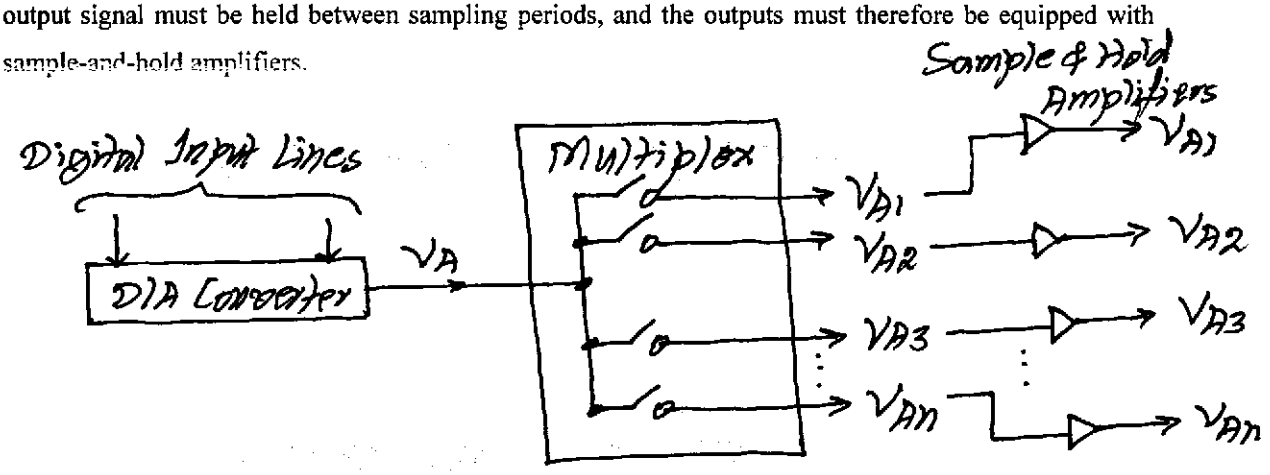
The first method is, simply to use one D/A converter for each signal (as shown in the following Fig). This has the advantage that, each signal to be decoded is held in its register and the analog output

voltage is then held fixed. The digital input li9nes are connected in parallel to each converter. The proper converter is then selected for decoding, by the select lines.



Decoding a Number of Signals - Channel Selection Method

The second method involves the use of only one D/A converter and switching its output. This is multiplexing; and such a system is shown in the following Fig. The disadvantage here is that, the analog output signal must be held between sampling periods, and the outputs must therefore be equipped with sample-and-hold amplifiers.

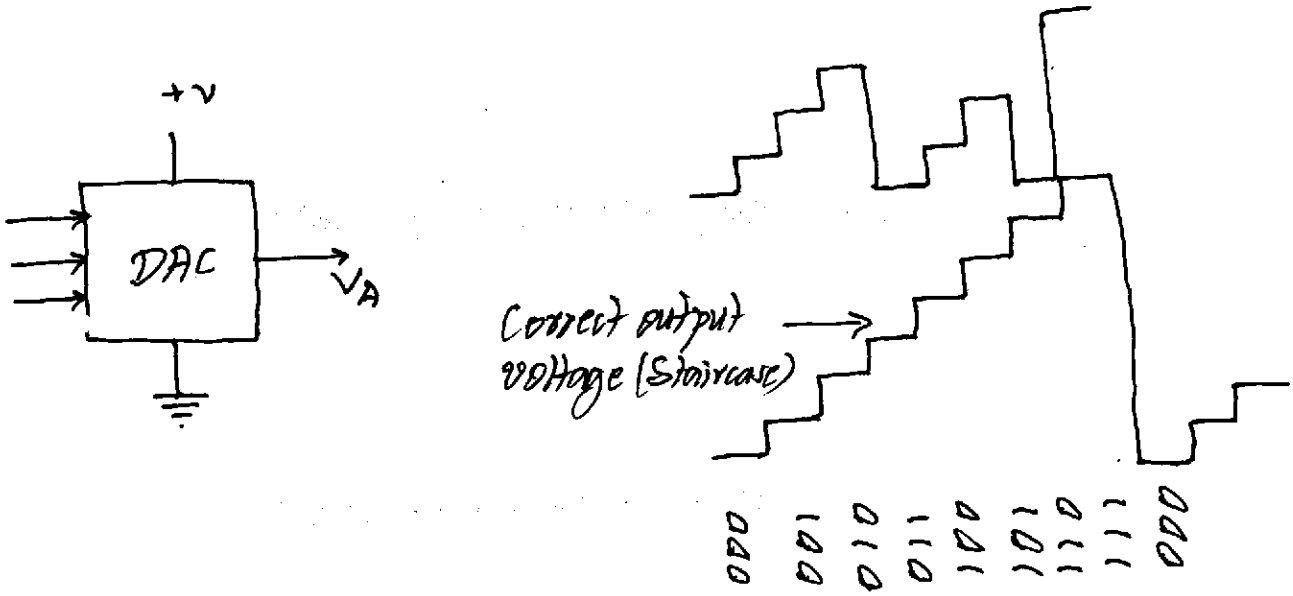


Decoding a Number of Signals - Multiplex Method

D/A Converter Testing: Two simple, but important tests that can be performed to check the proper operation of the D/A converter are the *study-state accuracy test* and the *monotonicity test*.

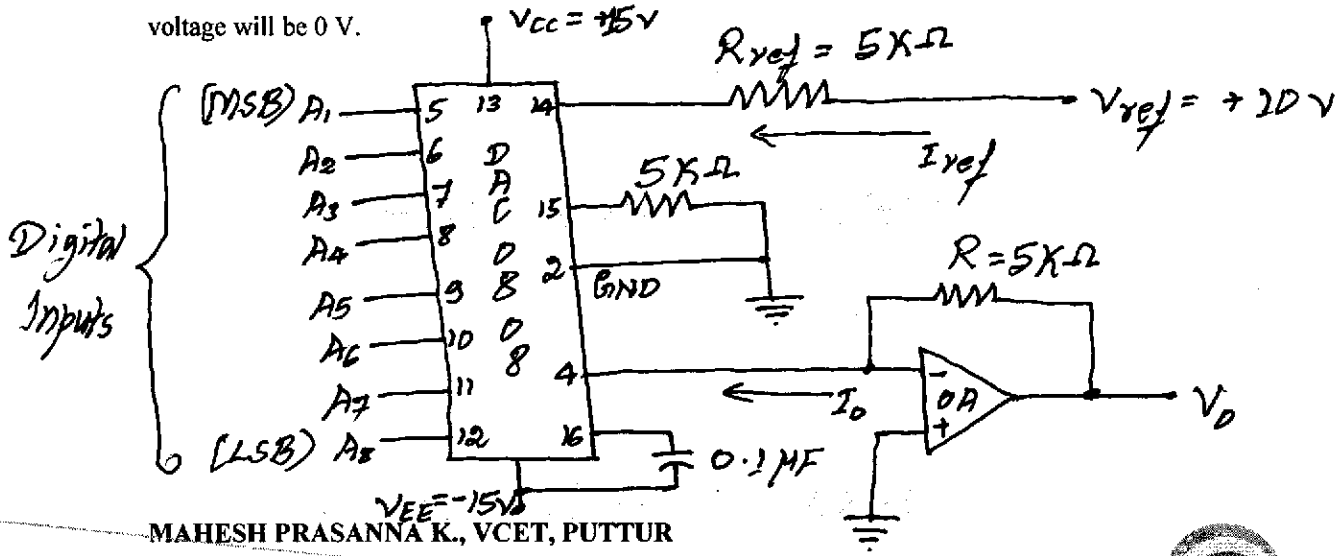
- The study-state accuracy test involves setting a known digital number in the input register, measuring the analog output with an accurate meter, and comparing with the theoretical value.

- Monotonicity test means, checking that the output voltage increases regularly as the input digital signal increases. This can be accomplished by using a counter as the digital input signal and observing the analog output voltage on an oscilloscope. For proper monotonicity, the output waveform should be a perfect staircase waveform (as shown below). The steps of the staircase waveform must be equally spaced and of the exact same amplitude. Missing steps, steps of different amplitude, or steps in a downward fashion indicate malfunctions (as shown below).



Monotonicity Test: Correct Output & Irregular Output Voltage Waveform

Available D/A Converters: D/A converters with 6-, 8-, 10-, 12-, 16-bit resolution are available. An inexpensive and very popular D/A converter is the DAC0808 – an 8-bit D/A converter, available from National Semiconductors. In the following Fig, a DAC0808 is connected to provide a full-scale output voltage of V0 = +10 V, when all 8 digital inputs are 1s. If the eight digital inputs are all 0s, the output voltage will be 0 V.



Two DC power supply voltages are required for the DAC0808: V_{CC} = +15 V and V_{EE} = –15 V. The 0.1 μF capacitor is to prevent unwanted circuit oscillations, and to isolate any variations in V_{EE}. Pin 2 is ground and pin 15 is also referenced to ground through a resistor.

The output of the D/A converter on pin 4 has a very limited voltage range (+0.5 to –0.6 V). This pin is designed to provide an output current, I_0. The minimum current is 0.0 mA, and the maximum current is I_{ref}. This reference current is established with the resistor at pin 14 and the reference voltage as;

$$I_{ref} = {}^{V_{ref}}/_{R_{ref}} \quad ----------(1)$$

The D/A converter output current I_0 is given as;

$$I_0 = I_{ref}\left(\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \ldots + \frac{A8}{256}\right) \quad ----------(2)$$

where, A1, A2, A3, . . . , A8 are the digital input levels (1 or 0).

The output voltage is given as; $V_0 = I_0 * R \quad ----------(3)$

Substituting equations (1) and (2) into (3), we get;

$$V_0 = {}^{V_{ref}}/_{R_{ref}}\left(\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \ldots + \frac{A8}{256}\right) * R$$

If R = R_{ref}, we get;

$$V_0 = V_{ref}\left(\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \ldots + \frac{A8}{256}\right)$$

Suppose, all the digital inputs are all 0s; then,

$$V_0 = V_{ref}\left(\frac{0}{2} + \frac{0}{4} + \frac{0}{8} + \ldots + \frac{0}{256}\right) = 0.0\,Vdc$$

Suppose, all the digital inputs are all 1s; then,

$$V_0 = V_{ref}\left(\frac{1}{2} + \frac{1}{4} + \frac{1}{8} + \ldots + \frac{1}{256}\right) = V_{ref}\left(\frac{255}{256}\right) = 0.996 * V_{ref}$$

Problem: *For a DA0808, A1 is high, A2 is high, A5 is high, and A7 is high. The other digital inputs are all 0s. What is the output voltage V_0?*

Solution:

$$V_0 = V_{ref}\left(\frac{1}{2} + \frac{1}{4} + \frac{1}{32} + \frac{1}{128}\right) = 10 * 0.789 = 7.89\,V$$

D/A ACCURACY AND RESOLUTION:

Two very important aspects of the D/A converter are the resolution and the accuracy of the conversion. The *accuracy of the D/A converter* is primarily a function of the accuracy of the precision resistors used in the ladder and the precision of the reference voltage supply used. *Accuracy* is a measure of how close the actual output voltage is to the theoretical output value.

For example, suppose that the theoretical output voltage for a particular input should be +10 V. An accuracy of 10 % means that, the actual output voltage must be somewhere between +9 and +11 V. Similarly, if the actual output voltage were somewhere between +9.9 and +10.1 V, this would be an accuracy of 1 %.

Resolution defines the smallest increment in voltage that can be distinguished. Resolution is primarily a function of the number of bits in the digital input signal; that is, the smallest increment in output voltage is determined by the LSB.

For example, in a 4-bit system, using ladder, the LSB has a weight of $\frac{1}{16}$. This means that, the smallest increment in the output voltage is $\frac{1}{16}$ of the input voltage. If we assume that, this 4-bit system has input voltage levels of +16 V; (since has a weight of $\frac{1}{16}$) a change in LSB results in a change of 1 V in the output. Thus, the output voltage changes in steps of 1 V.

Hence, this converter can be used to represent analog voltages from 0 to +15 V in 1-V increments. But, this converter can not be used to resolve voltages into increments smaller than 1V. If we desire to produce +4.2 V, using this converter, the actual output voltage would be +4.0 V. This converter is not capable of distinguishing voltages finer than 1 V, which is the resolution of the converter.

If we want to represent voltages to a finer resolution, we would have to use a converter with more input bits. For example, the LSB of a 10-bit converter has a weight of 1/1024. If this converter has a +10 V full-scale output, the resolution is approximately, $+10 * \frac{1}{1024} = 10$ mV.

Problem: *What is the resolution of a 9-bit D/A converter which uses a ladder network? What is the resolution expressed as a percentage? If the full-scale output voltage of this converter is +5 V, what is resolution in volts?*

Solution: The LSB in a 9-bit D/A converter has a weight of $\frac{1}{512}$. Thus, this converter has a resolution of 1 part in 512.

The resolution expressed in percentage is $\frac{1}{512} * 100$ percent = 0.2 %.

The voltage resolution is obtained by multiplying the weight of the LSB by the full-scale output voltage. Thus, the resolution in volts is: $\frac{1}{512} * 5 = 10$ mV.

Problem: *How many bits are required at the input of a converter, if it is necessary to resolve voltage to 5 mV and the ladder has +10 V full-scale?*

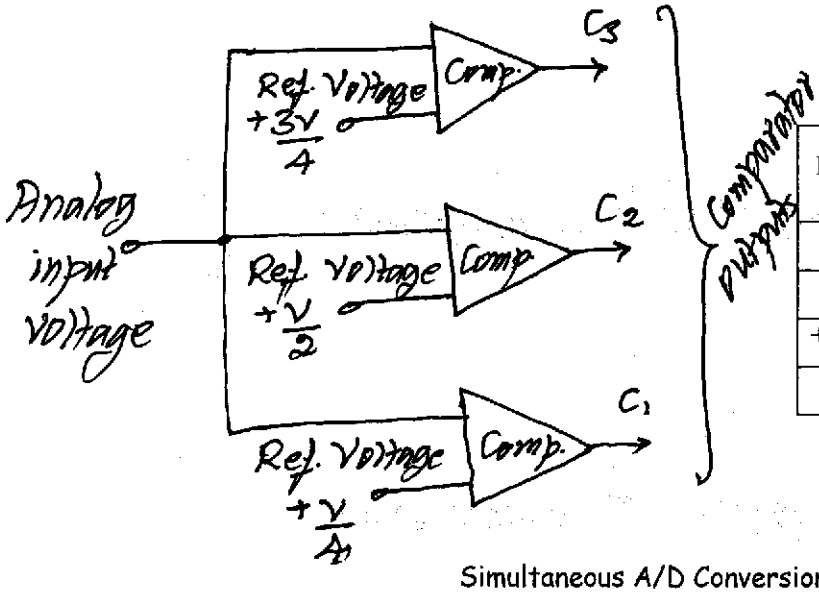
Solution: The LSB of an 11-bit D/A converter has a resolution of $\frac{1}{2048}$. This would provide a resolution at the output of $\frac{1}{2048} * 10 = +5$ mV.

A/D CONVERTER:

The process of converting an analog voltage into an equivalent digital signal is known as *analog-to-digital (A/D) conversion.*

A/D CONVERTER – SIMLUTANEOUS CONVERSION METHOD:

The simultaneous method of A/D conversion is based on the use of a number of comparator circuits. One such system using three comparators is shown in the following Fig.

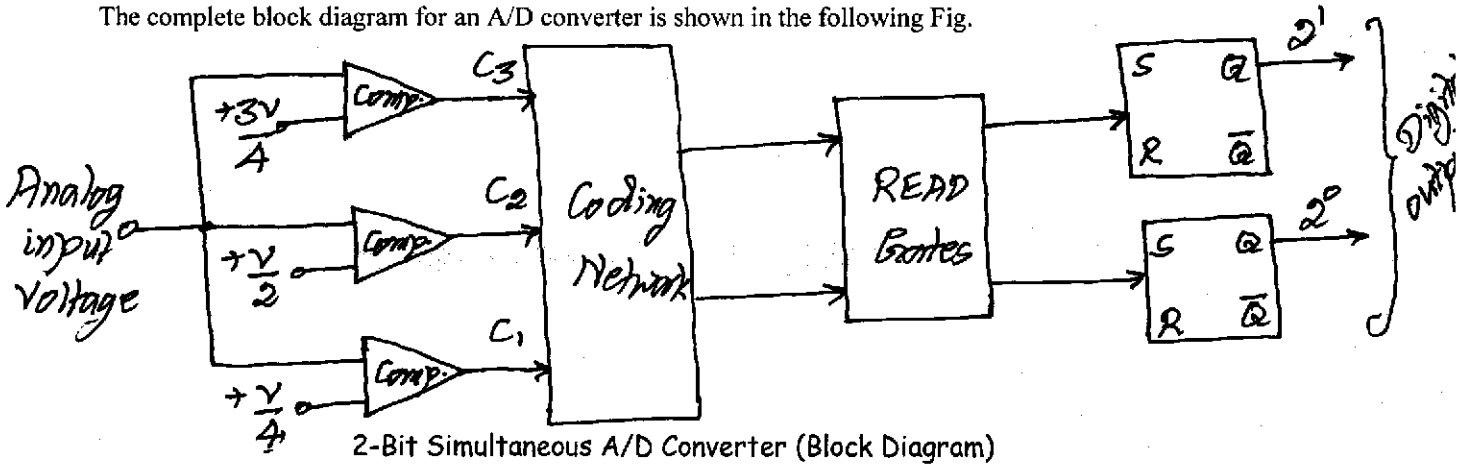


Input Voltage	Comparator Outputs		
	C_1	C_2	C_3
0 to +V/4	Low	Low	Low
+V/4 to +V/2	High	Low	Low
+V/2 to +3V/4	High	High	Low
+3V/4 to +V	High	High	High

Simultaneous A/D Conversion

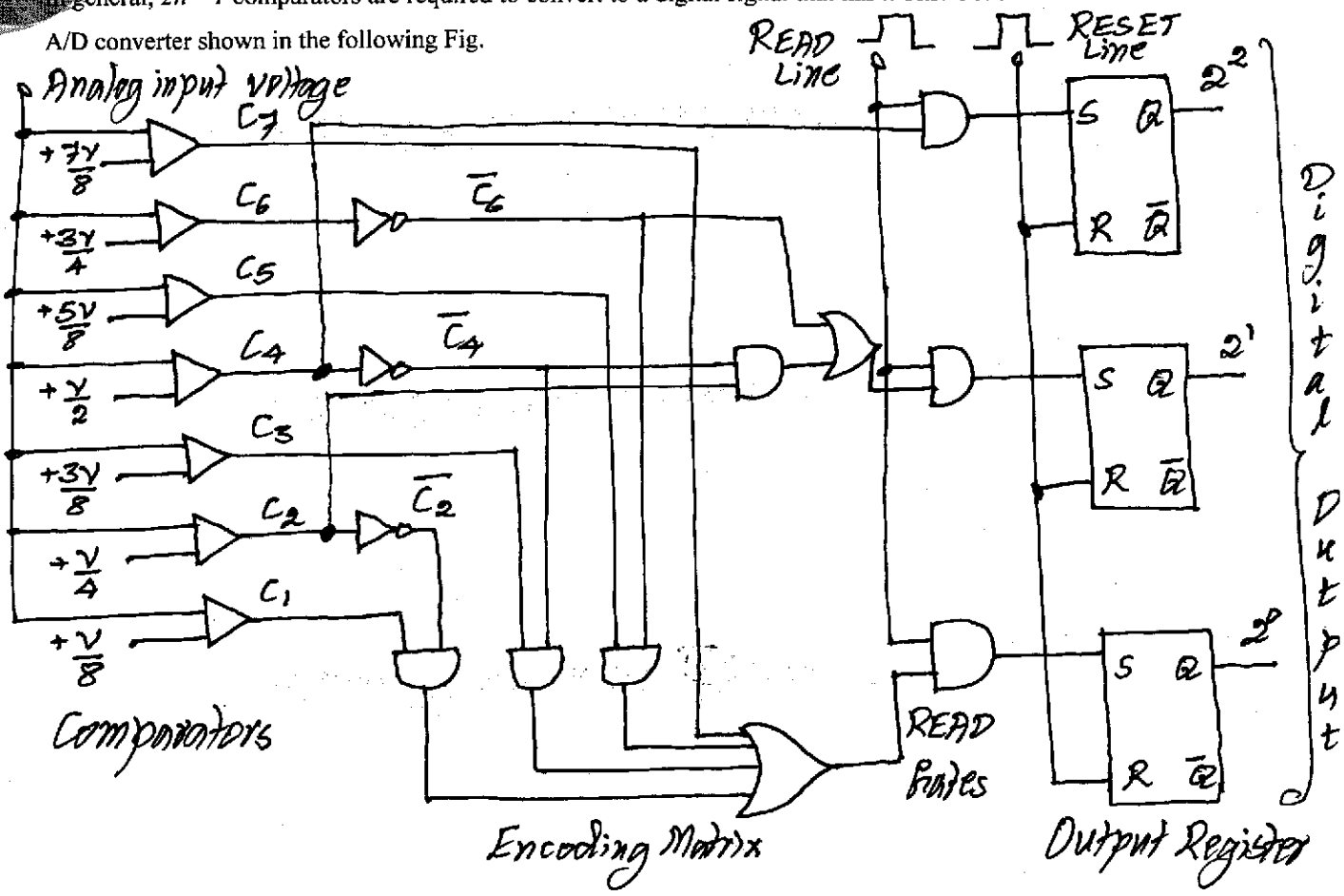
The analog signal to be digitized serves as one of the inputs to each comparator. The second input is a standard reference voltage. The system is capable of accepting an analog input voltage between 0 and +V. If the analog signal exceeds the reference voltage to any comparator, that comparator turns on. The comparator output levels for the various ranges of input voltages are summarized in the Table given above.

The complete block diagram for an A/D converter is shown in the following Fig.



2-Bit Simultaneous A/D Converter (Block Diagram)

In general, $2n - 1$ comparators are required to convert to a digital signal that has n bits. Consider the 3-bit A/D converter shown in the following Fig.



3-Bit Simultaneous A/D Converter

The coding network accepts seven input levels and encodes them into 3-bit binary number. Operation of the coding network can be understood by the Table of outputs given below.

Input Voltage	Comparator Level							Binary Output		
	C_1	C_2	C_3	C_4	C_5	C_6	C_7	2^2	2^1	2^0
0 to V/8	Low	Low	Low	Low	Low	Low	Low	0	0	0
V/8 to V/4	High	Low	Low	Low	Low	Low	Low	0	0	1
V/4 to 3V/8	High	High	Low	Low	Low	Low	Low	0	1	0
3V/8 to V/2	High	High	High	Low	Low	Low	Low	0	1	1
V/2 to 5V/8	High	High	High	High	Low	Low	Low	1	0	0
5V/8 to 3V/4	High	High	High	High	High	Low	Low	1	0	1
3V/4 to 7V/8	High	High	High	High	High	High	Low	1	1	0
7V/8 to V	High	High	High	High	High	High	High	1	1	1

Logic Table for the 3-Bit Simultaneous A/D Converter

The 2^2 bit is easiest to determine, since it must be high whenever C_4 is high.

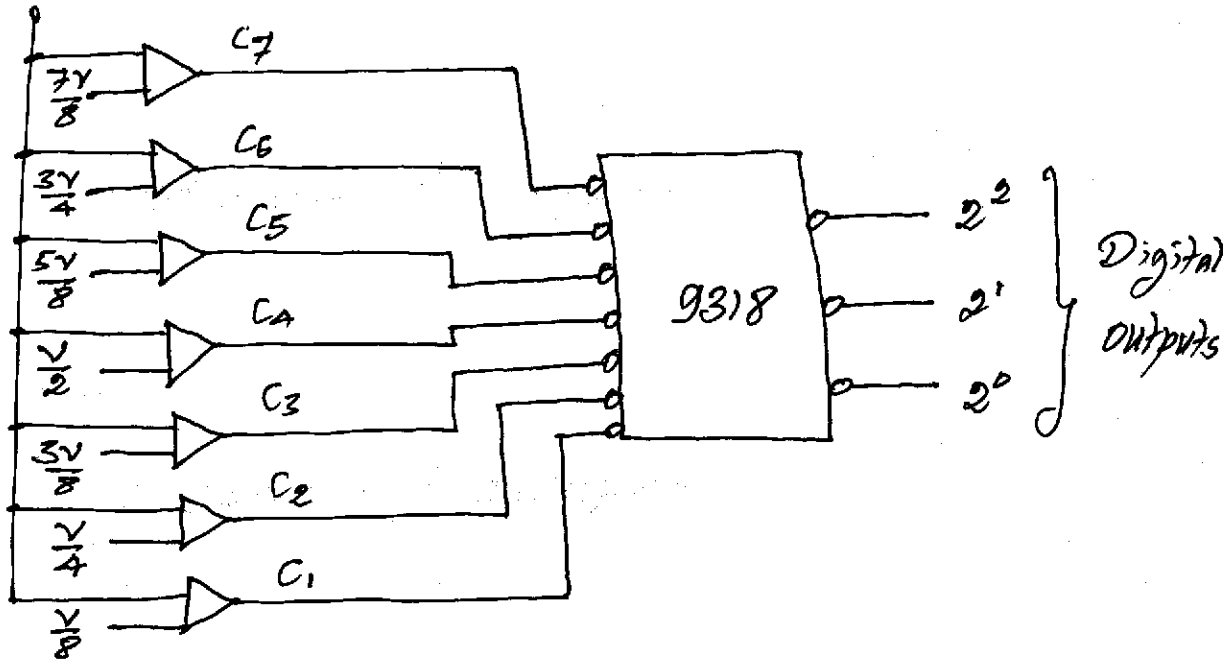
The 2^1 bit must be high whenever C_2 is high and $\bar{C}_4$ is high, or whenever C_6 is high. Hence, we can write; $2^1 = C_2\bar{C}_4 + C_6$.

In the similar manner; $2^0 = C_1\bar{C}_2 + C_3\bar{C}_4 + C_5\bar{C}_6 + C_7$.

The transfer of data from the encoding matrix into the register must be carried out in two steps:

- ✓ A positive RESET pulse to reset all the flip-flops low
- ✓ A positive READ pulse allows the proper READ gates to go high and thus transfer the digital information into the flip-flops.

A convenient application for a 9318 priority encoder is to use it to replace all the digital logic shown in the above Fig, as follows.



3-Bit Simultaneous A/D Converter Using 9318 Priority Encoder

Advantages:

- o The construction of a simultaneous A/D converter is quite straightforward and relatively easy to understand.
- o This method is simple and is capable of having extremely fast conversion rates. Hence, this type of converter is frequently called as a *flash converter*.

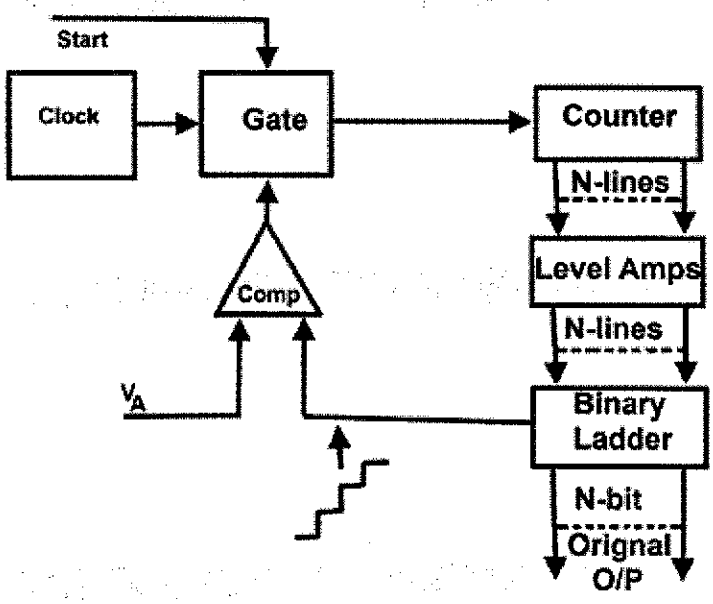
Disadvantages:

- As the number of bits in the desired digital system increases, the number of comparators increases rapidly $(2^n - 1)$.

Example: The Motorola MC10319 – an 8-bit flash A/D converter.

A/D CONVERTER – COUNTER METHOD:

A higher-resolution A/D converter using only one comparator could be constructed if a variable reference voltage is available. The following Fig shows the block diagram for a counter-type A/D converter.



Counter Type A/D Converter

First, the n-bit counter is reset to all 0s. When a signal appears on the START line, the gate opens and the clock pulses are allowed to pass through to the input of the counter. The counter advances through its normal binary sequence, and the staircase waveform is generated at the output of the ladder. This waveform is applied to one side of the comparator, and the analog input voltage (which is to be digitized) is applied to the other side. When the reference voltage equals (or exceeds) the input analog voltage, the gate is closed, the counter stops, and the conversion is complete. The number stored in the counter is now the digital equivalent of the analog input voltage.

Advantages: The counter-type A/D converter provides a very good method for digitizing to a high resolution. This method is much simpler than the simultaneous method for high resolution.

Disadvantages: The conversion time required is longer. Since, the counter always begins at zero and counts through its normal binary sequence, as many as 2^n counts may be necessary before conversion is complete. The *average conversion time is, $2^n/2$ or 2^{n-1} counts.*

Problem: *Suppose that, a counter-type A/D converter for 8-bit is driven by a 500 KHz clock. Fine (a) the maximum conversion time; (b) the average conversion time; (c) the maximum conversion rate.*

Solution:

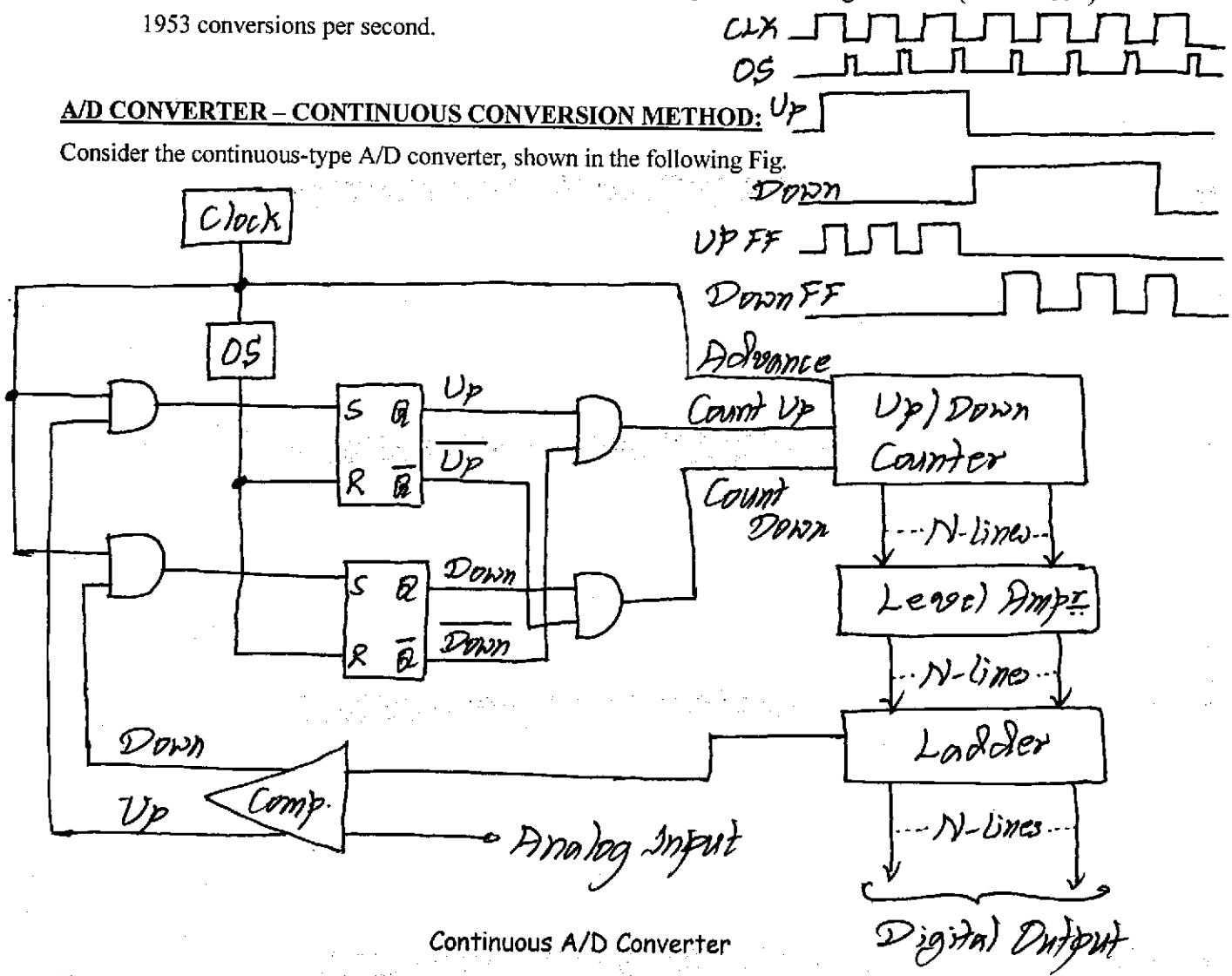
(a) An 8-bit converter has a maximum of 2^8 = 256 counts. With a 500 KHz clock, the counter advances at the rate of 1 count each (1/500 K) 2 μs. To advance 256 counts, the counter requires $256 * 2 * 10^{-6} = 512$ μs.

(b) The average conversion time is one-half the maximum conversion time. Thus, it is ½ * 512 μs = 0.256 ms.

(c) The maximum conversion rate is determined by the longest conversion time. Since the converter has the maximum conversion time of 0.512 ms, it is capable of making at least $1/(0.512 * 10^{-3})$ = 1953 conversions per second.

A/D CONVERTER – CONTINUOUS CONVERSION METHOD:

Consider the continuous-type A/D converter, shown in the following Fig.



Continuous A/D Converter

The output of the ladder is fed into a comparator which has two outputs. When the analog voltage is more positive than the ladder output, the *up* count of the comparator is high. When the analog voltage is more negative than the ladder output, the *down* count of the comparator is high.

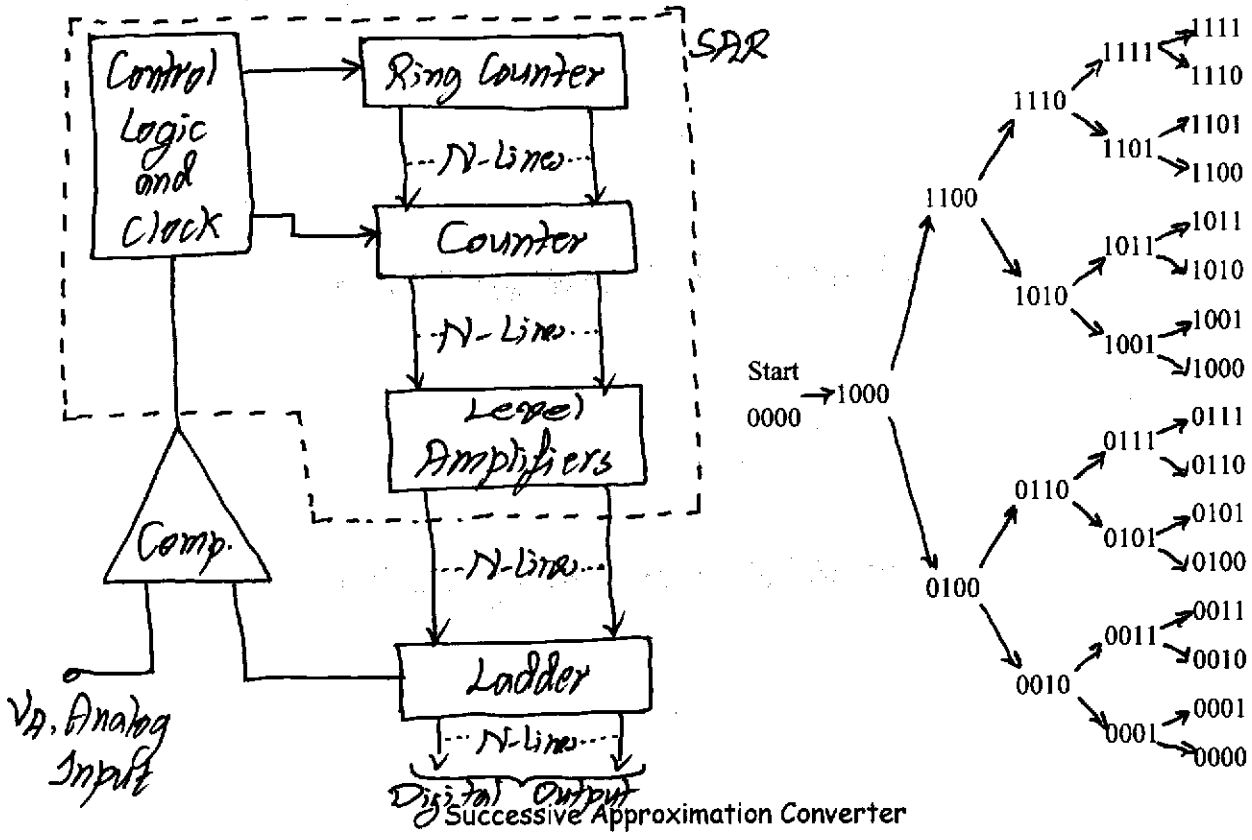
If the *up* output of the comparator is high, the AND gate at the input of the *up* flip-flop is open, and the first time the clock goes positive, the *up* flip-flop is set, and the counter will advance one count.

counter can advance only one count, since the output of the one-shot (OS) resets both *up* and *down* flip-flops just after the clock goes low.

As long as the *up* output of the comparator is high, the converter continuous to operate one conversion cycle at a time. At the point, where the ladder voltage becomes more positive than the analog input voltage, the *up* output of the comparator goes low and the *down* output of the comparator goes high. The conversion then goes through a count-down conversion cycle.

A/D TECHNIQUES – SUCCESSIVE APPROXIMATION:

The block diagram for successive approximation converter is shown in the following Fig.



Successive Approximation Converter

The converter operates by successively dividing the voltage ranges in half. The counter first resets to all 0s, and the MSB is then set. The output of the ladder produces an analog equivalent of MSB and is compared with the analog input (which is to be digitized).

If the comparator output is low, means, the ladder output is greater than the analog input. Hence, the MSB will be cleared and the next bit will be set. If the comparator output is high, means, the ladder output is less than the analog input. Hence, the MSB is set to the next position. The process goes on until all the bits are tried.

Advantages: High speed and better resolution.

Example: ADC0804: 8-bit CMOS microprocessor compatible successive-approximation A/D converter.

DUAL-SLOPE A/D CONVERSION:

Self Study.

A/D ACCURACY AND RESOLUTION:

Self Study.

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